Bipolar Junction Transistors (BJTs)

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INTRODUCTION

- The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source,

- The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits, which led to electronics changing the way we work,

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- the reliability of BJT circuits under severe environmental conditions makes them the dominant device in automotive electronics, an important and still-growing area.

- The BJT is still the preferred device in very demanding analog circuit applications, both integrated and discrete. This is especially true in very-high-frequency applications, such as radio frequency (RF) circuits for wireless systems.

- bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors.

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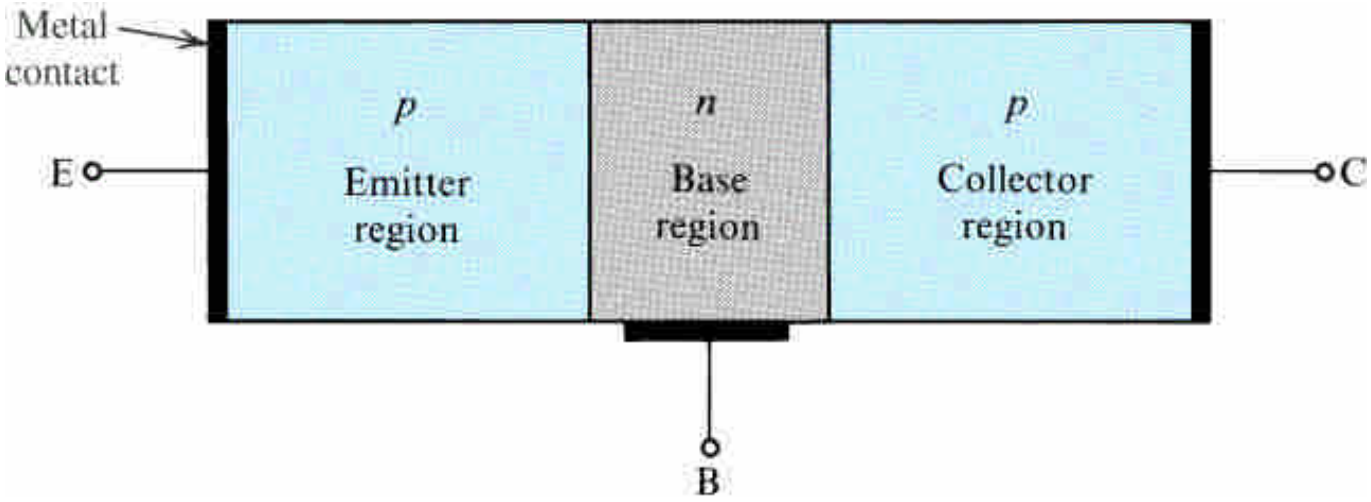

Figure 5.2 A simplified structure of the *pnp* transistor.

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5.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

- As shown in Fig. 5.1, the BJT consists of three semiconductor regions: the emitter region (*n* type), the base region (*p* type), and the collector region (*n* type). Such a transistor is called an *npn* transistor. Another transistor, a dual of the *Npn* as shown in Fig. 5.2,

- the terminals labeled **Emitter** (E), **base** (B), and **collector** (C).

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- The transistor consists of two *pn* junctions, the **emitter–base junction** (EBJ) and the **collector–base junction** (CBJ).

- The **active mode,** which is also called forward active mode, is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the **Cutoff** and the **saturation modes.** The **reverse active** (or inverse active) mode has very limited application

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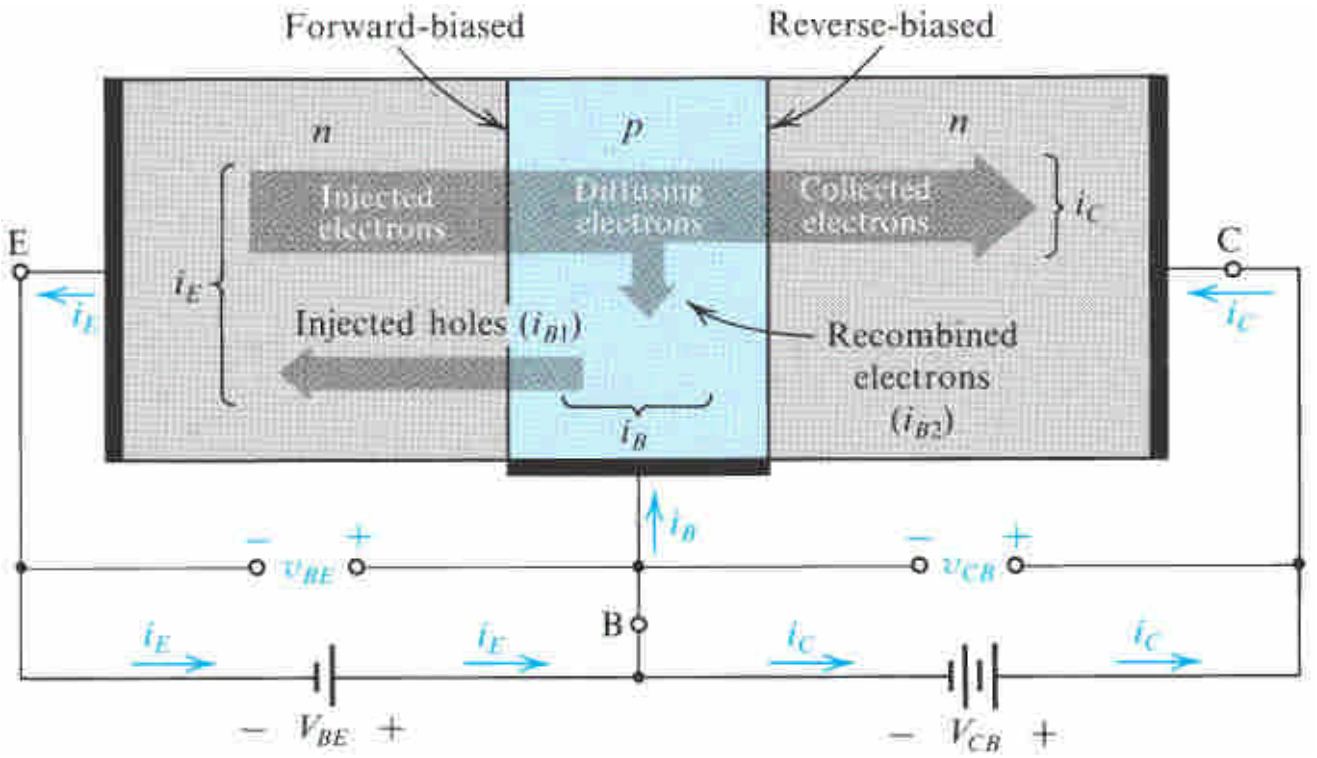

Figure 5.3 Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

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5.1.2 Operation of the *npn* Transistor in the Active Mode

- Two external voltage sources are used to establish the required bias conditions for active-mode operation. The voltage V_{BE} causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward-biasing the emitter–base junction. The collector–base voltage V_{CB} causes the *n*-type collector to be higher in potential than the *p*-type base, thus reverse-biasing the collector–base junction.

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Current Flow

- The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter.
- the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

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- The direction of i_E is “out of” the emitter lead, which is in the direction of the hole current and opposite to the direction of the electron current, with the emitter current i_E being equal to the sum of these two components.

- the emitter current will be dominated by the electron component.

- Let us now consider the electrons injected from the emitter into the base. These electrons will be **minority carriers** in the *p* -type base region.

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- The electron concentration will be highest [denoted by $n_p(0)$] at the emitter side and lowest (zero) at the collector side. As in the case of any forward-biased *pn* junction (Section 3.7.5), the concentration $n_p(0)$ will be proportional to e^{v_{BE}/V_T}

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \qquad (5.1)$$

where is the thermal equilibrium value of the minority-carrier (electron) concentration in the base region, v_{BE} is the forward base–emitter bias voltage, and V_T is the thermal voltage, which is equal to approximately 25 mV at room temperature

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- This electron diffusion current I_n is directly proportional to the slope of the straight-line concentration profile,

$$I_n = A_E q D_n \frac{dn_p(x)}{dx} = A_E q D_n \left(-\frac{n_p(0)}{W} \right) \qquad (5.2)$$

Where A_E is the cross-sectional area of the base–emitter junction ,q is the magnitude of the electron charge, D_n is the electron diffusivity in the base, and W is the effective width of the base.

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The Collector Current

- most of the diffusing electrons will reach the boundary of the collector–base depletion region. Because the collector is more positive than the base (by v_{CB} volts),

$$i_C = I_S e^{v_{BE}/V_T} \qquad (5.3)$$

where the **saturation current** I_S is given by

$$I_S = A_E q D_n n_{p0}/W$$

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Substituting $n_{p0} = n_i^2 / N_A$ where n_i is the intrinsic carrier density and N_A is the doping concentration of the base, we can express I_S as

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \qquad (5.4)$$

- An important observation to make here is that the magnitude of i_C is independent of v_{CB}.

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The Base Current

- The base current i_B is composed of two components. The first component i_{B1} is due to the holes injected from the base region into the emitter region. This current component is proportional to

$$i_{B1} = \frac{A_E q D_p n_i^2}{N_D L_p} e^{v_{BE}/V_T} \qquad (5.5)$$

where D_p is the hole diffusivity in the emitter, L_p is the hole diffusion length in the emitter, and N_D is the doping concentration of the emitter.

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- The second component of base current, i_{B2}, is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process.

the current i_{B2} must supply the base with a positive charge equal to Q_n every τ_b seconds,

$$i_{B2} = \frac{Q_n}{\tau_b} \tag{5.6}$$

$$Q_n = A_E q \times \tfrac{1}{2} n_p(0) W$$

replacing n_{p0} by n_i^2/N_A gives

$$Q_n = \frac{A_E q W n_i^2}{2N_A} e^{v_{BE}/V_T} \tag{5.7}$$

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$$i_{B2} = \frac{1}{2}\frac{A_E q W n_i^2}{\tau_b N_A} e^{v_{BE}/V_T} \tag{5.8}$$

$$i_B = I_S\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n \tau_b}\right) e^{v_{BE}/V_T} \tag{5.9}$$

Comparing Eqs. (5.3) and (5.9), we see that i_B can be expressed as a fraction of i_C as follows:

$$i_B = \frac{i_C}{\beta} \tag{5.10}$$

$$i_B = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T} \tag{5.11}$$

$$\beta = 1\Big/\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n \tau_b}\right) \tag{5.12}$$

the constant β is called the **common-emitter current gain.**

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The Emitter Current

$$i_E = i_C + i_B \tag{5.13}$$

$$i_E = \frac{\beta + 1}{\beta} i_C \tag{5.14}$$

$$i_E = \frac{\beta + 1}{\beta} I_S e^{v_{BE}/V_T} \tag{5.15}$$

$$i_C = \alpha i_E \tag{5.16}$$

$$\alpha = \frac{\beta}{\beta + 1} \tag{5.17}$$

$$i_E = (I_S/\alpha) e^{v_{BE}/V_T} \tag{5.18}$$

$$\beta = \frac{\alpha}{1 - \alpha} \tag{5.19}$$

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α is a constant (for the particular transistor) that is less than but very close to unity. For instance, if β = 100, then $\alpha \doteq$ 0.99.

- Small changes in α correspond to very large changes in β.

α is called the **common-base current gain.**

- because α and β characterize the operation of the BJT in the “forward active” mode, they are often denoted α_F and β_F

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5.1.3 Structure of Actual Transistors

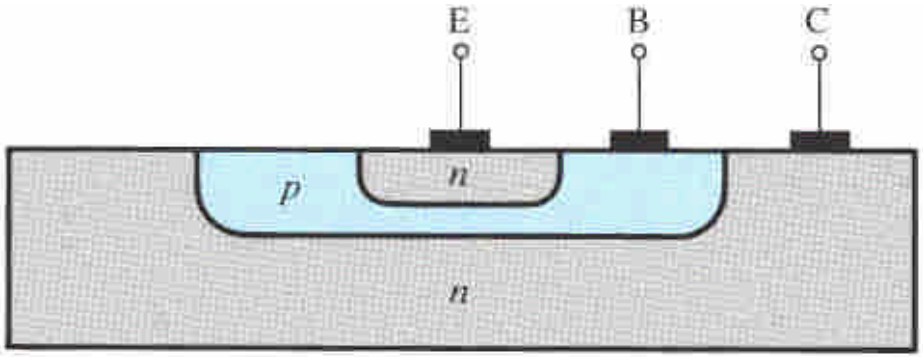

Figure 5.6 Cross-section of an *npn* BJT.

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5.1.4 The Ebers-Moll (EM) Model

- this composite model can be used to predict the operation of the BJT *in all of its possible modes*.

$$i_E = i_{DE} - \alpha_R i_{DC} \tag{5.21}$$

$$i_C = -i_{DC} + \alpha_F i_{DE} \tag{5.22}$$

$$i_B = (1-\alpha_F) i_{DE} + (1-\alpha_R) i_{DC} \tag{5.23}$$

$$i_{DE} = I_{SE}(e^{v_{BE}/V_T} - 1) \tag{5.24}$$

$$i_{DC} = I_{SC}(e^{v_{BC}/V_T} - 1) \tag{5.25}$$

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$$i_E = \left(\frac{I_S}{\alpha_F}\right)(e^{v_{BE}/V_T} - 1) - I_S(e^{v_{BC}/V_T} - 1) \tag{5.26}$$

$$i_C = I_S(e^{v_{BE}/V_T} - 1) - \left(\frac{I_S}{\alpha_R}\right)(e^{v_{BC}/V_T} - 1) \tag{5.27}$$

$$i_B = \left(\frac{I_S}{\beta_F}\right)(e^{v_{BE}/V_T} - 1) + \left(\frac{I_S}{\beta_R}\right)(e^{v_{BC}/V_T} - 1) \tag{5.28}$$

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{5.29}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{5.30}$$

$$i_E \cong \left(\frac{I_S}{\alpha_F}\right)e^{v_{BE}/V_T} + I_S\left(1 - \frac{1}{\alpha_F}\right) \tag{5.31}$$

$$i_C \cong I_S e^{v_{BE}/V_T} + I_S\left(\frac{1}{\alpha_R} - 1\right) \tag{5.32}$$

$$i_B \cong \left(\frac{I_S}{\beta_F}\right)e^{v_{BE}/V_T} - I_S\left(\frac{1}{\beta_F} + \frac{1}{\beta_R}\right) \tag{5.33}$$

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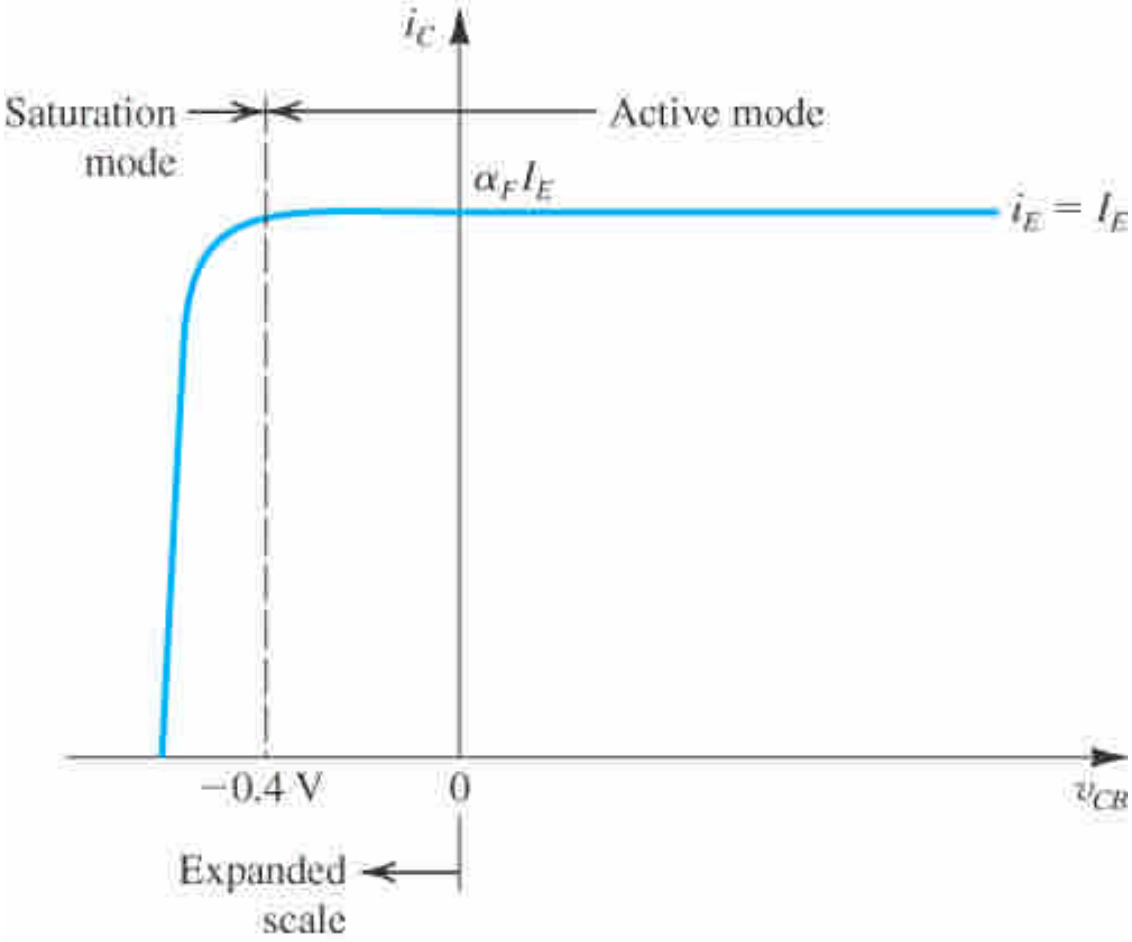

Figure 5.9 The i_C–v_{CB} characteristic of an *npn* transistor fed with a constant emitter current I_E. The transistor enters the saturation mode of operation for $v_{CB} < -0.4$ V, and the collector current diminishes.

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5.1.5 Operation in the Saturation Mode

- Figure 5.9 indicates that as v_{CB} is lowered below approximately 0.4 V, the BJT enters the saturation mode of operation.

- Increasing v_{CB} in the negative direction—that is, increasing the forward-bias voltage of the CBJ—reduces i_C

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5.1.6 The *pnp* Transistor

- The *pnp* transistor operates in a manner similar to that of the *npn* device described above. Figure 5.11 shows a *pnp* transistor biased to operate in the active mode. Here the voltage V_{EB} causes the *p*-type emitter to be higher in potential than the *n*-type base, thus forward-biasing the base–emitter junction. The collector–base junction is reverse-biased by the voltage V_{BC}, which keeps the *p*-type collector lower in potential than the *n*-type base.

- current in the *pnp* device is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage V_{EB}.

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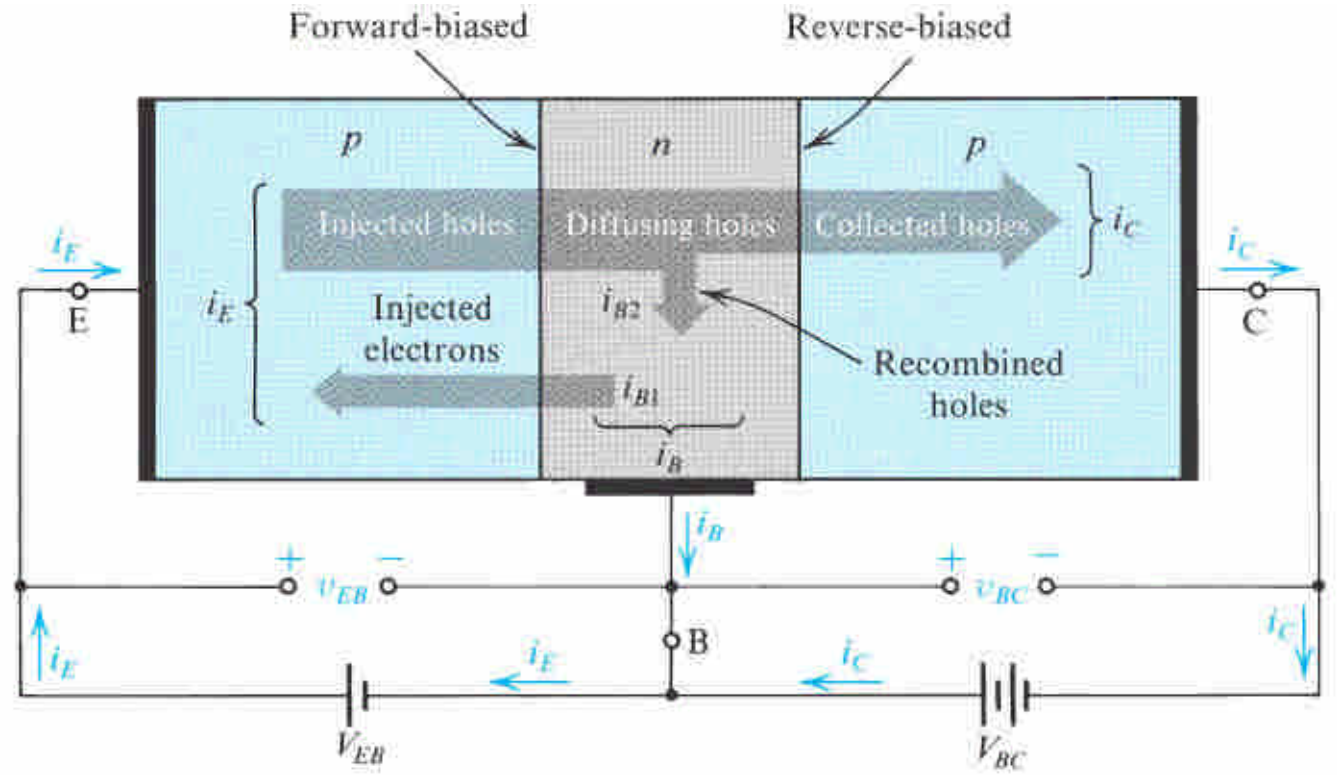

Figure 5.11 Current flow in a *pnp* transistor biased to operate in the active mode.

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5.2 CURRENT-VOLTAGE CHARACTERISTICS

5.2.1 Circuit Symbols and Conventions

- Figure 5.13(a) shows the symbol for the *npn* transistor; the *pnp* symbol is given in Fig. 5.13(b).
- This arrowhead points in the direction of normal current flow in the emitter, which is also the forward direction of the base–emitter junction.
- Figure 5.14 shows *npn* and *pnp* transistors biased to operate in the active mode.

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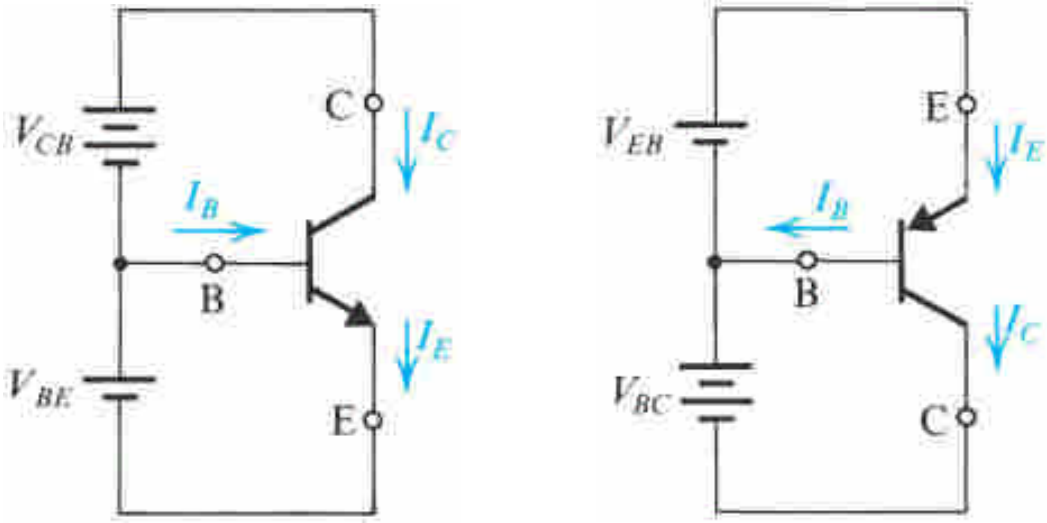

Figure 5.14 Voltage polarities and current flow in transistors biased in the active mode.

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- an *npn* transistor whose EBJ is forward biased will operate in the active mode *as long as the collector voltage does not fall below that of the base by more than approximately 0.4 V*. Otherwise, the transistor leaves the active mode and enters the saturation region of operation.

- In a parallel manner, the *pnp* transistor will operate in the active mode *if the EBJ is forward biased and the collector voltage is not allowed to rise above that of the base by more than 0.4 V or so*. Otherwise, the CBJ becomes forward biased, and the *pnp* transistor enters the saturation region of operation.

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TABLE 5.2 Summary of the BJT Current-Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1-\alpha) i_E = \frac{i_E}{\beta + 1}$$

$$i_C = \beta i_B \qquad i_E = (\beta + 1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta + 1}$$

V_T = thermal voltage $= \dfrac{kT}{q} \cong 25$ mV at room temperature

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EXAMPLE 5.1

The transistor in the circuit of Fig. 5.15(a) has $\beta = 100$ and exhibits a v_{BE} of 0.7 V at $i_C = 1$ mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.

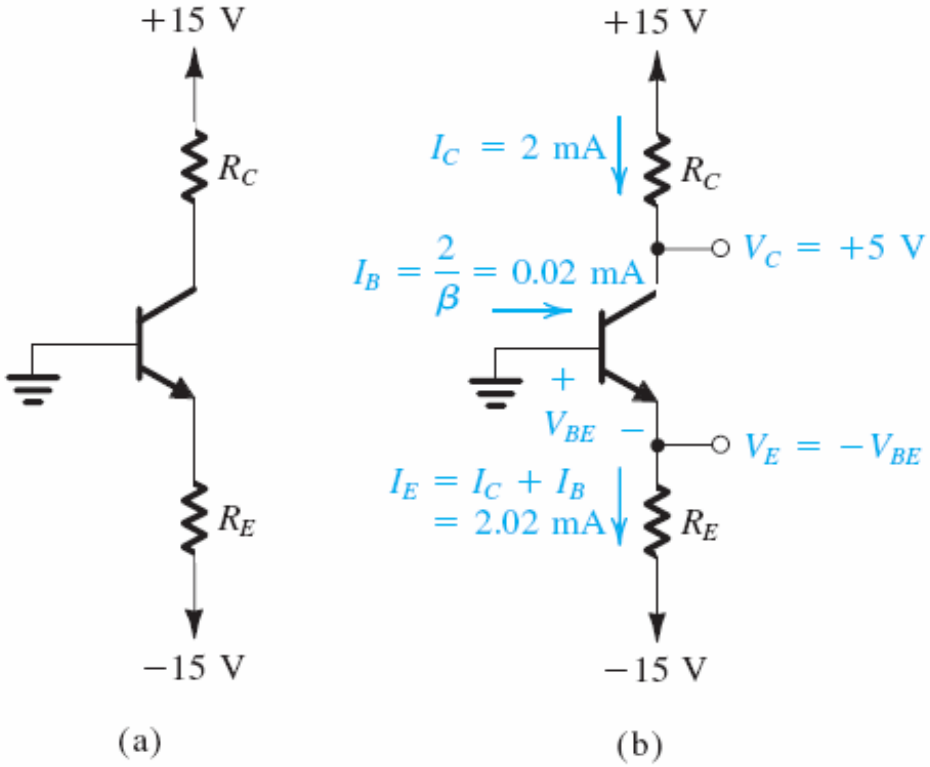

FIGURE 5.15 Circuit for Example 5.1.

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Solution

Refer to Fig. 5.15(b). We note at the outset that since we are required to design for $V_C = +5$ V, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage $V_C = +5$ V the voltage drop across R_C must be $15 - 5 = 10$ V. Now, since $I_C = 2$ mA, the value of R_C should be selected according to

$$R_C = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since $v_{BE} = 0.7$ V at $i_C = 1$ mA, the value of v_{BE} at $i_C = 2$ mA is

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.717 \text{ V}$$

Since the base is at 0 V, the emitter voltage should be

$$V_E = -0.717 \text{ V}$$

For $\beta = 100$, $\alpha = 100/101 = 0.99$. Thus the emitter current should be

$$I_E = \frac{I_C}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

Now the value required for R_E can be determined from

$$R_E = \frac{V_E - (-15)}{I_E}$$

$$= \frac{-0.717 + 15}{2.02} = 7.07 \text{ k}\Omega$$

This completes the design. We should note, however, that the calculations above were made with a degree of accuracy that is usually neither necessary nor justified in practice in view, for instance, of the expected tolerances of component values. Nevertheless, we chose to do the design precisely in order to illustrate the various steps involved.

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5.2.2 Graphical Representation of Transistor Characteristics

- Figure 5.16 shows the *iC–vBE* characteristic, which is the exponential relationship

$$i_C = I_S e^{v_{BE}/V_T}$$

which is identical (except for the value of constant *n*) to the diode *i–v* relationship. The i_E–v_{BE} and i_B–v_{BE} characteristics are also exponential but with different scale currents: for i_E, and for i_B.

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- For v_{BE} smaller than about 0.5 V, the current is negligibly small.

- over most of the normal current range v_{BE} lies in the range of 0.6 V to 0.8 V. we normally will assume that *VBE* 0.7 V,

- As in silicon diodes, the voltage across the emitter–base junction decreases by about 2 mV for each rise of 1°C in temperature,

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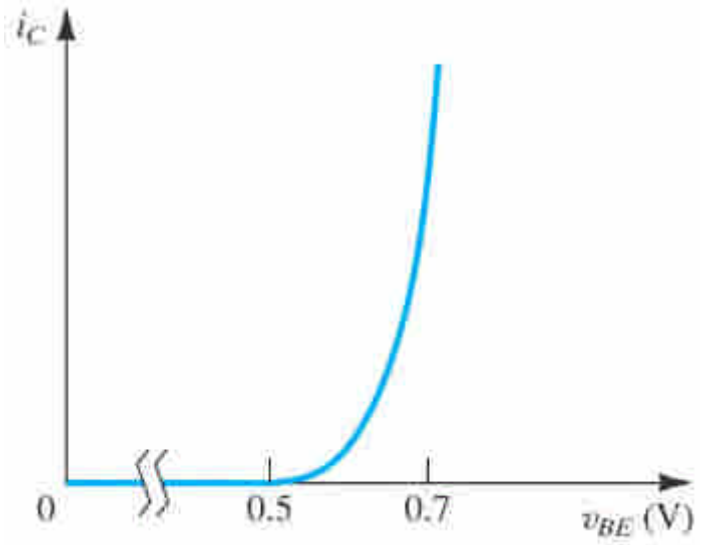

Figure 5.16 The i_C–v_{BE} characteristic for an *npn* transistor.

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The Common-Base Characteristics

- In the active region of operation, obtained $v_{cb} \geqq$ -0.4V for or so, the i_C–v_{CB} curves deviate from our expectations in two ways.

- First, the curves are not horizontal straight lines but show a small positive slope, indicating that i_C *d*epends slightly on v_{CB} in the active mode. We shall discuss this phenomenon shortly.

- Second, at relatively large values of v_{CB}, the collector current shows a rapid increase, which is a breakdown phenomenon we will consider at a later stage.

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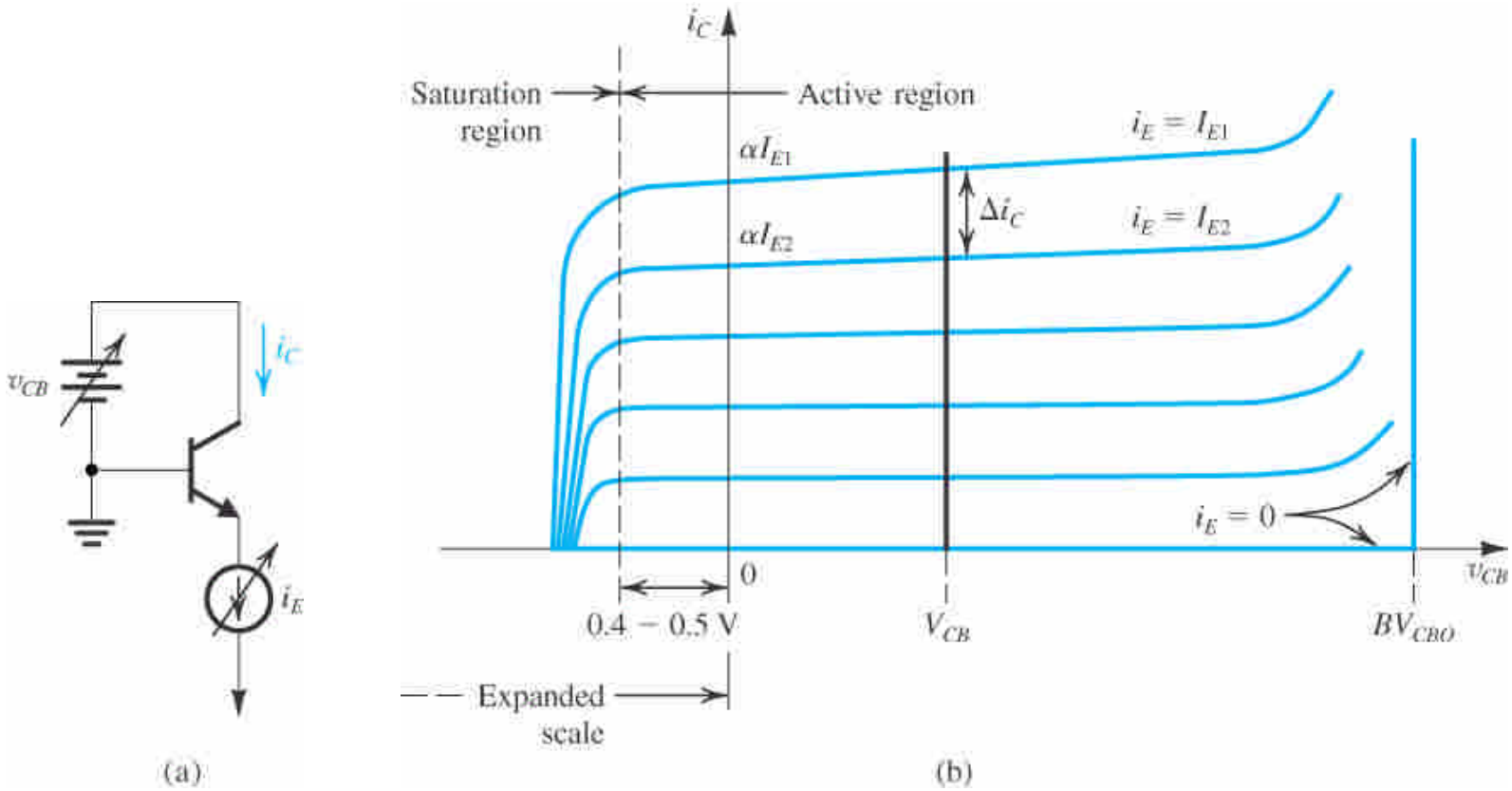

Figure 5.18 The i_C–v_{CB} characteristics of an *npn* transistor.

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5.2.3 Dependence of *iC* on the Collector Voltage—The Early Effect

- Fig. 5.19(a). The transistor is connected in the **common-emitter configuration**
- The result is the family of i_C–v_{CE} characteristic curves shown in Fig. 5.19(b) and known as **common-emitter characteristics.**
- when extrapolated, the characteristic lines meet at a point on the negative v_{CE} axis, at $v_{CE} = -V_A$. The voltage V_A, a positive number, is a parameter for the particular BJT, with typical values in the range of 50 V to 100 V. It is called the **Early voltage,**

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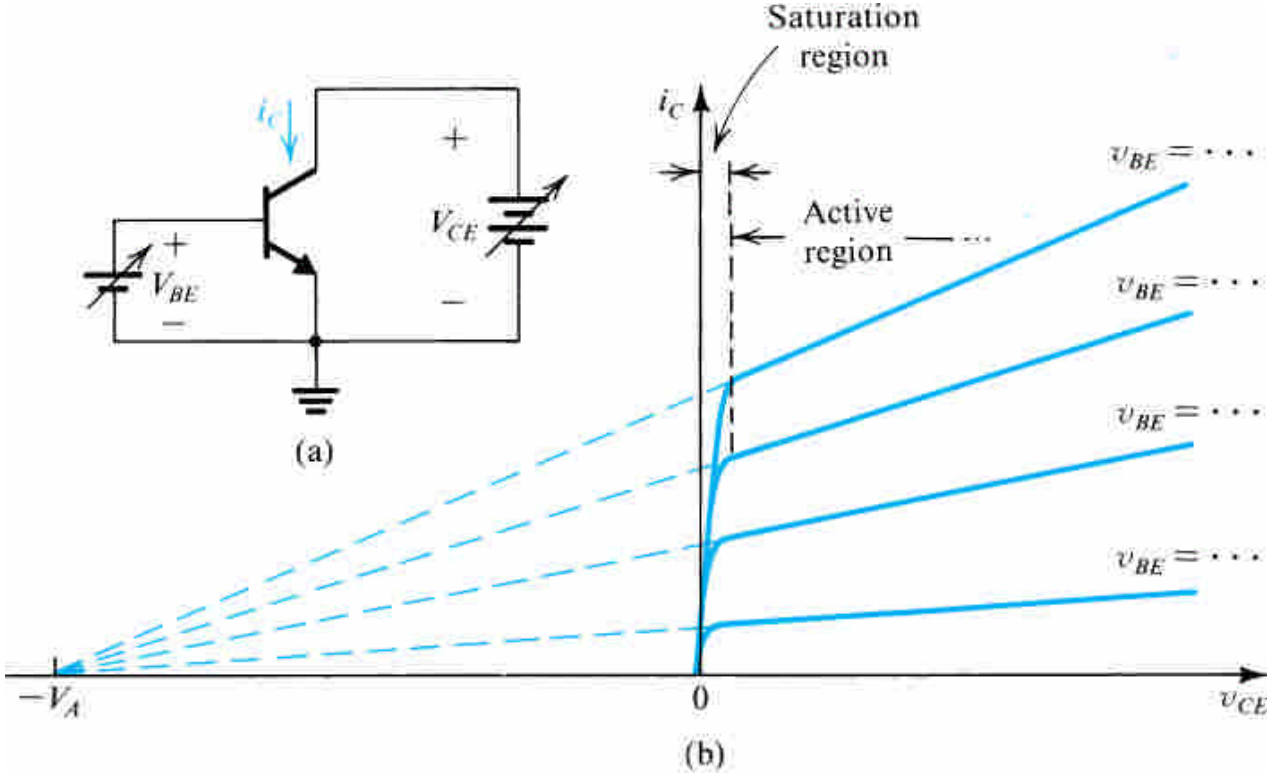

Figure 5.19 **(a)** Conceptual circuit for measuring the i_C–v_{CE} characteristics of the BJT. **(b)** The i_C–v_{CE} characteristics of a practical BJT.

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- At a given value of v_{BE}, increasing v_{CE} increases the reverse-bias voltage on the collector–base junction and thus increases the width of the depletion region of this junction (refer to Fig. 5.3). This in turn results in a decrease in the **effective base width** W.

- Recalling that I_S is inversely proportional to W (Eq. 5.4), we see that I_S will increase and that i_C increases proportionally. This is the Early effect.

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$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right) \qquad (5.36)$$

$$r_o = \frac{V_A + V_{CE}}{I_C} \qquad (5.38)$$

Alternatively, we can write

$$r_o = \frac{V_A}{I'_C} \qquad (5.38a)$$

where I'_c is the value of the collector current with the Early effect neglected

$$I'_C = I_S e^{V_{BE}/V_T} \qquad (5.38b)$$

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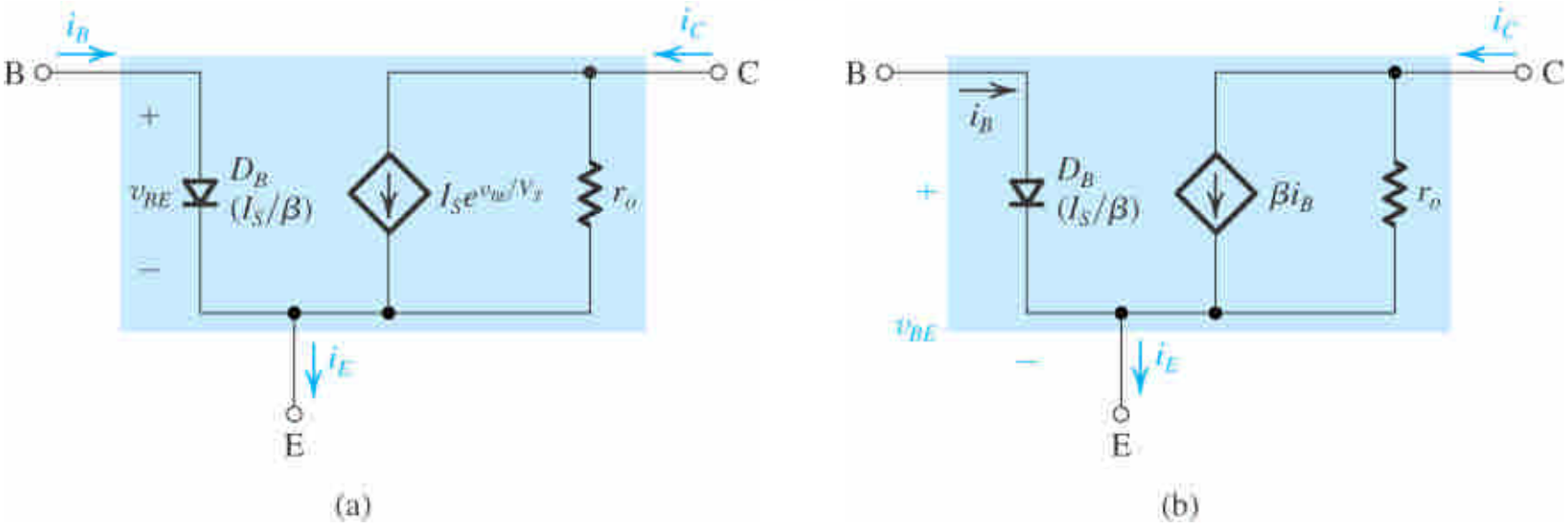

Figure 5.20 Large-signal equivalent-circuit models of an *npn* BJT operating in the active mode in the common-emitter configuration.

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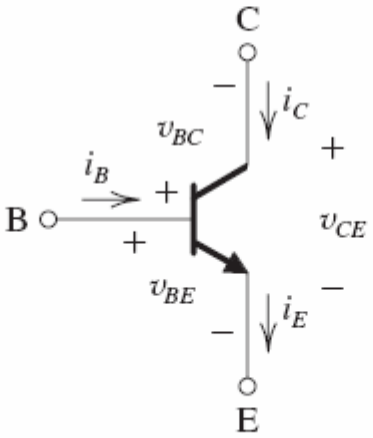
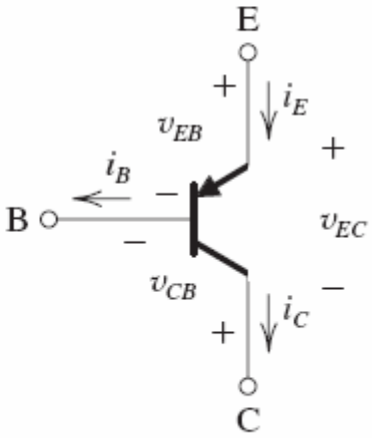
5.3 THE BJT AS AN AMPLIFIER AND AS A SWITCH

TABLE 5.3 Summary of the BJT Current-Voltage Characteristics

Circuit Symbol and Directions of Current Flow	*npn* Transistor	*pnp* Transistor
		

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Operation in the Active Mode (for Amplifier Application)

Conditions:

1. EBJ Forward Biased	$v_{BE} > V_{BEon}$; $V_{BEon} \cong 0.5$ V	$v_{EB} > V_{EBon}$; $V_{EBon} \cong 0.5$ V
	Typically, $v_{BE} = 0.7$ V	Typically, $v_{EB} = 0.7$ V
2. CBJ Reversed Biased	$v_{BC} \le V_{BCon}$; $V_{BCon} \cong 0.4$ V	$v_{CB} \le V_{CBon}$; $V_{CBon} \cong 0.4$ V
	$\Rightarrow v_{CE} \ge 0.3$ V	$\Rightarrow v_{EC} \ge 0.3$ V
Current-Voltage Relationships	■ $i_C = I_S e^{v_{BE}/V_T}$	■ $i_C = I_S e^{v_{EB}/V_T}$

- $i_B = i_C/\beta \quad \Leftrightarrow \quad i_C = \beta i_B$
- $i_E = i_C/\alpha \quad \Leftrightarrow \quad i_C = \alpha i_E$
- $\beta = \dfrac{\alpha}{1-\alpha} \quad \Leftrightarrow \quad \alpha = \dfrac{\beta}{\beta+1}$

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5.3.1 Large-Signal Operation—The Transfer Characteristic

- Figure 5.26(a) shows the basic structure (skeleton) of the most commonly used BJT amplifier, the **grounded-emitter** or **common-emitter (CE)** circuit.
- Resistor *RC* has $v_{BE}=v_I$, $v_O=v_{CE}$,two functions: to establish a desired dc bias voltage at the collector, and to convert the collector signal current i_c to an output voltage, v_{ce} or v_o.
- Figure 5.26(b) shows the voltage transfer characteristic of the CE circuit of Fig. 5.26(a).

$$v_O = v_{CE} = V_{CC} - R_C i_C \qquad (5.50)$$

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- since $v_{BE} = v_I$, the transistor will be effectively cutoff for $v_I < 0.5$ V or so. Thus, for the range $0 < v_I < 0.5$ V, i_C will be negligibly small, and v_O will be equal to the supply voltage V_{CC}

$$i_C \cong I_S e^{v_{BE}/V_T} = I_S e^{v_I/V_T}$$

$$v_O = V_{CC} - R_C I_S e^{v_I/V_T} \qquad (5.51)$$

In the saturation region, $v_{CE} = V_{CE\text{sat}}$,

$$I_{C\text{sat}} = \frac{V_{CC} - V_{CE\text{sat}}}{R_C} \qquad (5.52)$$

- When saturated, transistor can be thought of as a closed switch.On the other hand, when the BJT is cutoff, thus acts as an open switch

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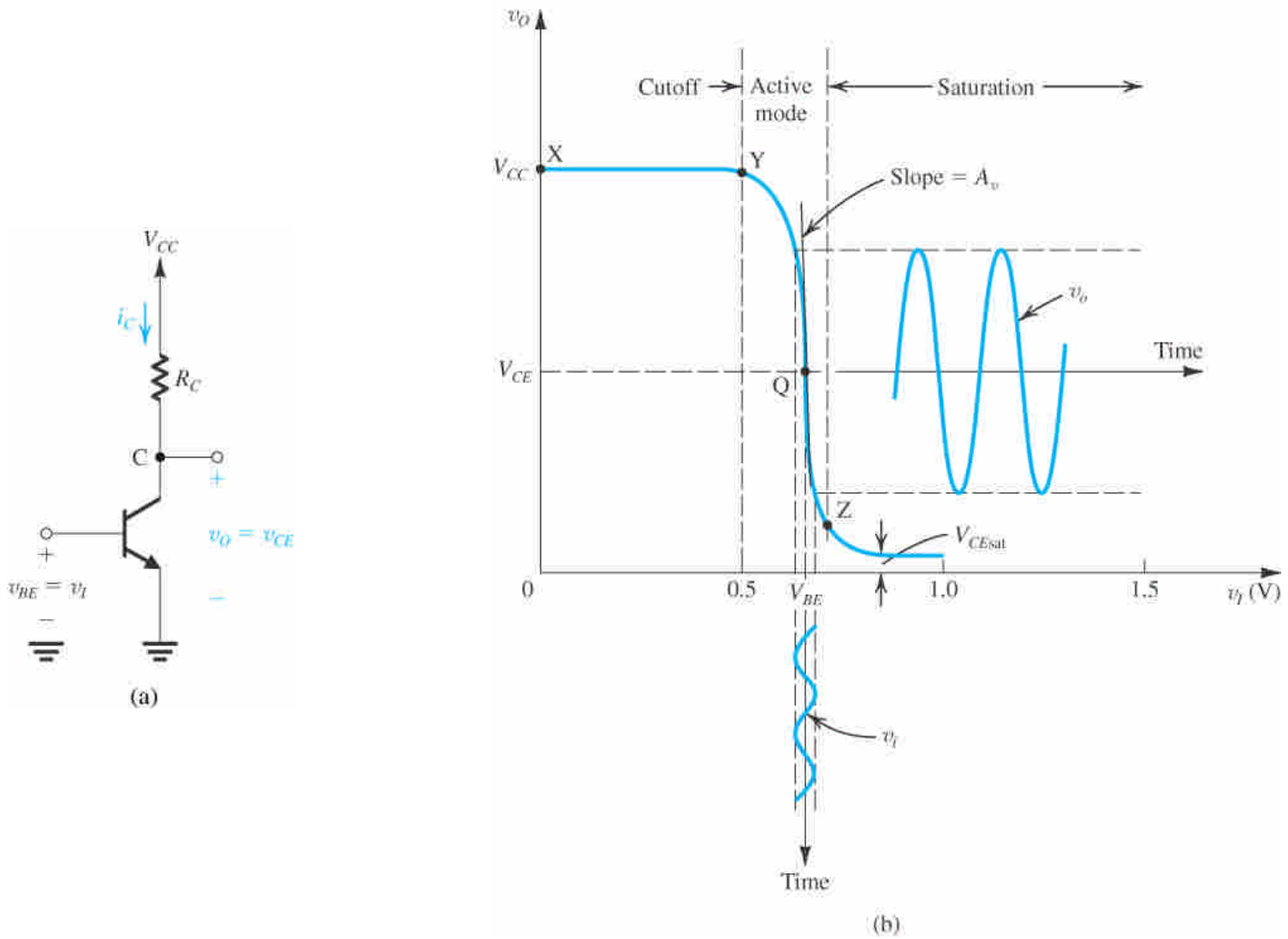

Figure 5.26 **(a)** Basic common-emitter amplifier circuit. **(b)** Transfer characteristic of the circuit in (a). The amplifier is biased at a point Q, and a small voltage signal v_i is superimposed on the dc bias voltage V_{BE}. The resulting output signal v_o appears superimposed on the dc collector voltage V_{CE}. The amplitude of v_o is larger than that of v_i by the voltage gain A_v.

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5.3.2 Amplifier Gain

- If the collector current at this value of V_{BE} is denoted I_C, that is

$$I_C = I_S e^{V_{BE}/V_T} \tag{5.53}$$

$$V_{CE} = V_{CC} - R_C I_C \tag{5.54}$$

- An expression for the small-signal gain A_v can be found by differentiating the expression in Eq. (5.51) and evaluating the derivative at point Q; that is, for $v_I = V_{BE}$,

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$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{BE}} \tag{5.55}$$

$$A_v = -\frac{1}{V_T} I_S e^{V_{BE}/V_T} R_C$$

Now, using Eq. (5.53) we can express A_v in compact form:

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T} \tag{5.56}$$

$$V_{RC} = V_{CC} - V_{CE} \tag{5.57}$$

$$A_v = -\frac{V_{CC} - V_{CE\text{sat}}}{V_T} \tag{5.58}$$

$$A_{v\text{max}} \cong -\frac{V_{CC}}{V_T} \tag{5.59}$$

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5.3.4 Operation as a Switch

- To operate the BJT as a switch, we utilize the cutoff and the saturation modes of operation.

- For v_I less than about 0.5 V, the transistor will be cutoff; thus $i_B = 0, i_C = 0$, and $v_C = V_{CC}$

- To turn the transistor on, we have to increase v_I above 0.5 V. In fact, for appreciable currents to flow, *vBE* should be about 0.7 V and v_I should be higher.

$$i_B = \frac{v_I - V_{BE}}{R_B} \qquad (5.60)$$

$$i_C = \beta i_B \qquad (5.61)$$

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which applies only when the device is in the active mode. This will be the case as long as the CBJ is not forward biased, that is, as long as $vC > vB - 0.4$ V,

- Eventually, v_C will become lower than v_B by 0.4 V, at which point the transistor leaves the active region and enters the saturation region. This **edge-of-saturation (EOS)** point is defined by

$$I_{C(\text{EOS})} = \frac{V_{CC} - 0.3}{R_C} \tag{5.63}$$

$$I_{B(\text{EOS})} = \frac{I_{C(\text{EOS})}}{\beta} \tag{5.64}$$

$$V_{I(\text{EOS})} = I_{B(\text{EOS})} R_B + V_{BE} \tag{5.65}$$

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- we shall usually assume that for a saturated transistor, $V_{CE\text{sat}} \cong 0.2$ V.

$$I_{C\text{sat}} = \frac{V_{CC} - V_{CE\text{sat}}}{R_C} \tag{5.66}$$

$$\beta_{\text{forced}} \equiv \frac{I_{C\text{sat}}}{I_B} \tag{5.67}$$

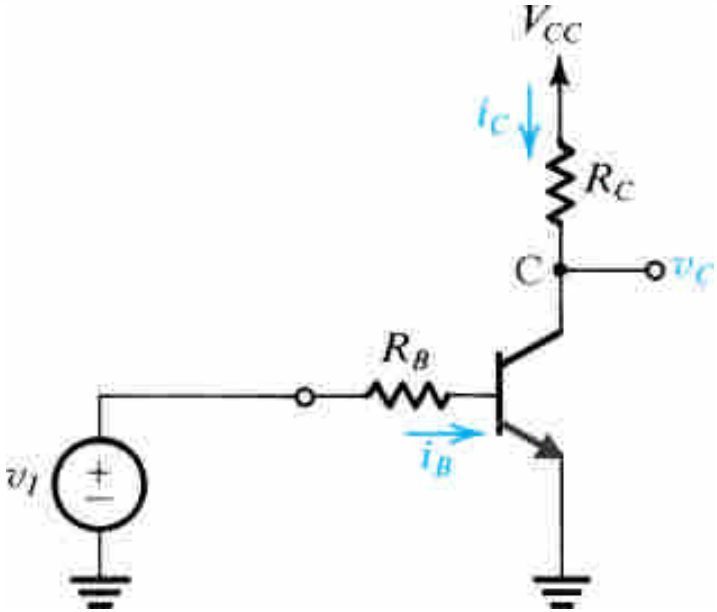

Figure 5.32 A simple circuit used to illustrate the different modes of operation of the BJT.

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5.4 BJT CIRCUITS AT DC

- In the following examples we will use the simple model in which, $|V_{BE}|$of a conducting transistor is 0.7 V and $|V_{CE}|$ of a saturated transistor is 0.2 V, and we will neglect the Early effect.
- procedure:

Assume that the transistor is operating in the active mode, and proceed to determine the various voltages and currents. Then check for consistency of the results with the assumption of active-mode operation; that is, is v_{CB} of an *npn* transistor greater than −0.4 V (or v_{CB} of a *pnp* transistor lower than 0.4 V)?

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- If the answer is yes, then our task is complete. If the answer is no, assume saturation-mode operation, and proceed to determine currents and voltages and to check for consistency of the results with the assumption of saturation-mode operation. Here the test is usually to compute the ratio and to verify that it is lower than the transistor β; i.e., $\beta_{\text{forced}} < \beta$

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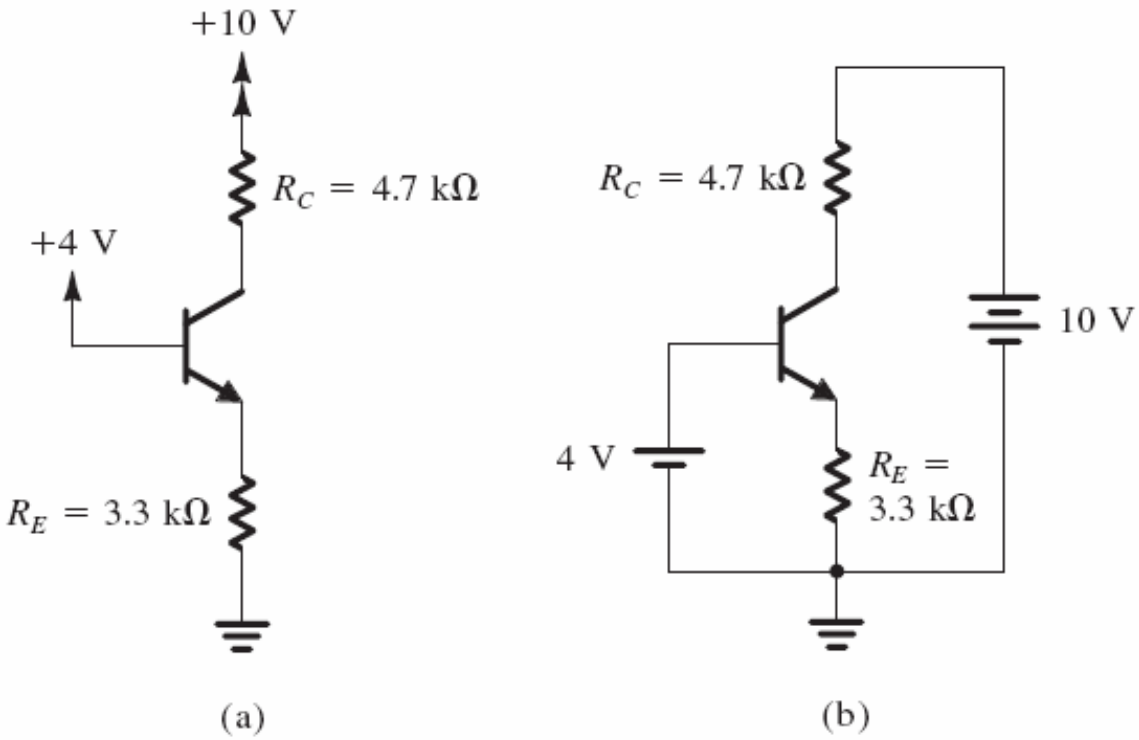
EXAMPLE 5.4

Consider the circuit shown in Fig. 5.34(a), which is redrawn in Fig. 5.34(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100.



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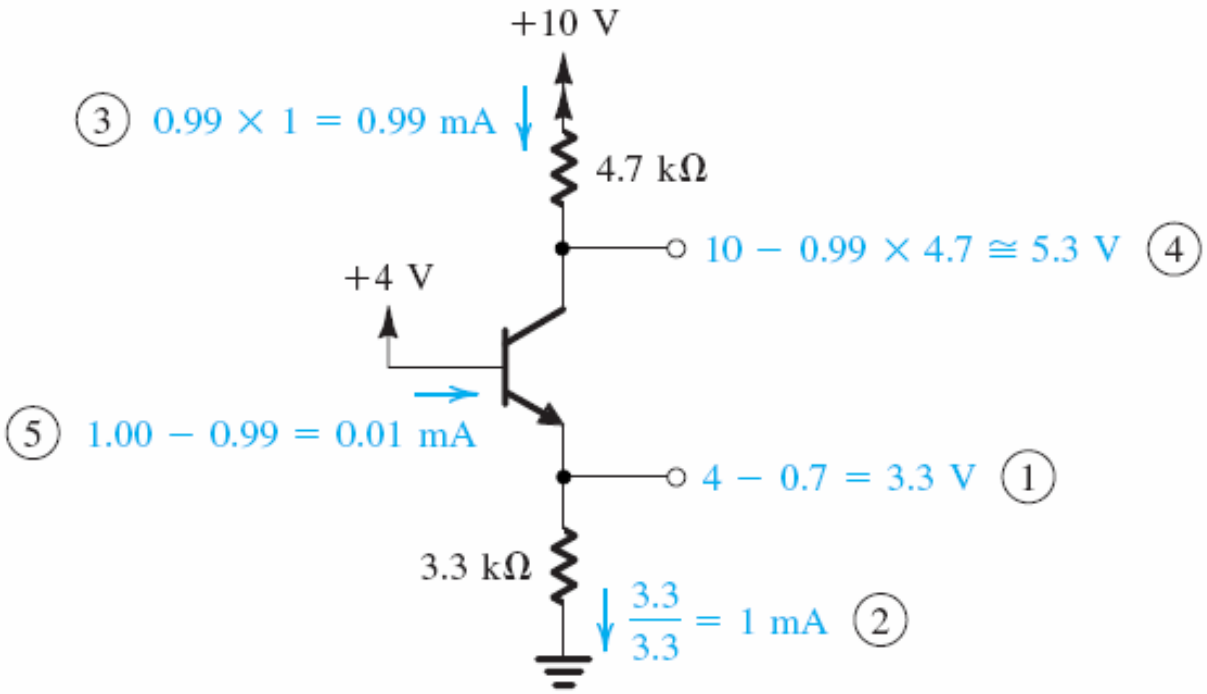

(c)

FIGURE 5.34 Analysis of the circuit for Example 5.4: **(a)** circuit; **(b)** circuit redrawn to remind the reader of the convention used in this book to show connections to the power supply; **(c)** analysis with the steps numbered.

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Solution

Glancing at the circuit in Fig. 5.34(a), we note that the base is connected to +4 V and the emitter is connected to ground through a resistance R_E. It therefore is safe to conclude that the base–emitter junction will be forward biased. Assuming that this is the case and assuming that V_{BE} is approximately 0.7 V, it follows that the emitter voltage will be

$$V_E = 4 - V_{BE} \simeq 4 - 0.7 = 3.3 \text{ V}$$

We are now in an opportune position; we know the voltages at the two ends of R_E and thus can determine the current I_E through it,

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

Since the collector is connected through R_C to the +10-V power supply, it appears possible that the collector voltage will be higher than the base voltage, which is essential for active-mode operation. Assuming that this is the case, we can evaluate the collector current from

$$I_C = \alpha I_E$$

The value of α is obtained from

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \simeq 0.99$$

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Thus I_C will be given by

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

We are now in a position to use Ohm's law to determine the collector voltage V_C,

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \simeq +5.3 \text{ V}$$

Since the base is at +4 V, the collector–base junction is reverse biased by 1.3 V, and the transistor is indeed in the active mode as assumed.

It remains only to determine the base current I_B, as follows:

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \simeq 0.01 \text{ mA}$$

Before leaving this example we wish to emphasize strongly the value of carrying out the analysis directly on the circuit diagram. Only in this way will one be able to analyze complex circuits in a reasonable length of time. Figure 5.34(c) illustrates the above analysis on the circuit diagram, with the order of the analysis steps indicated by the circled numbers.

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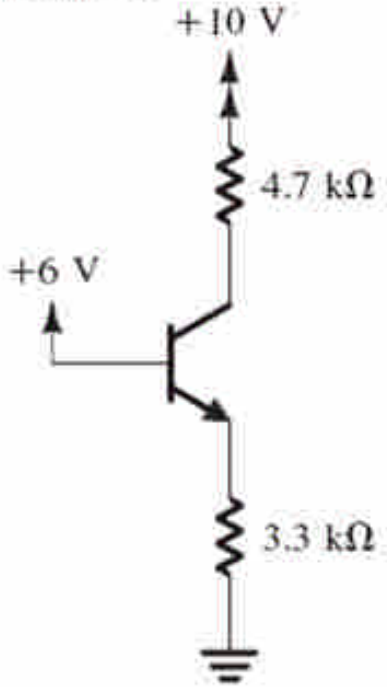
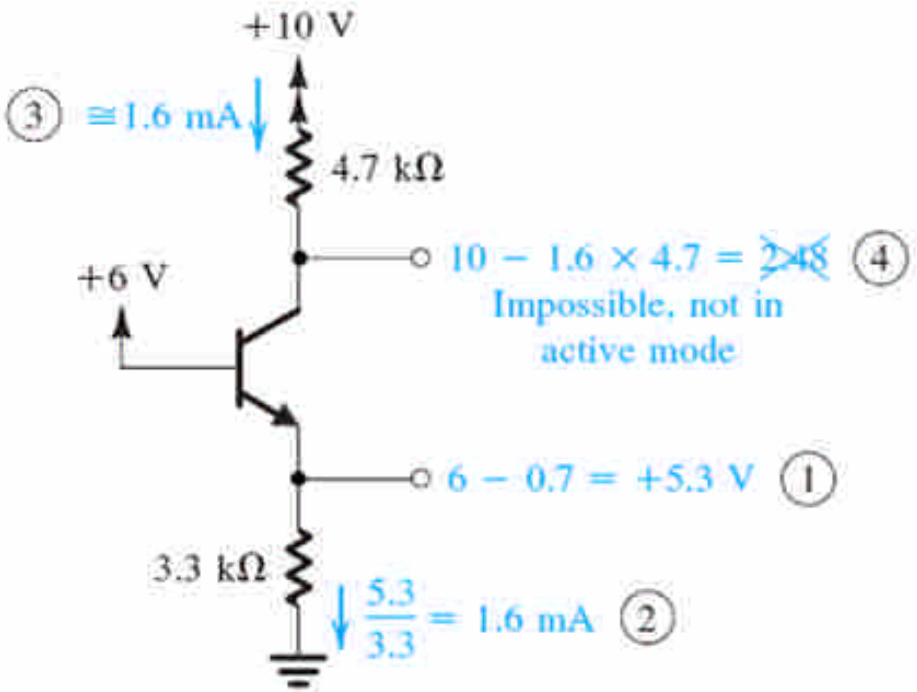
EXAMPLE 5.5

We wish to analyze the circuit of Fig. 5.35(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 5.34 except that the voltage at the base is now +6 V. Assume that the transistor β is specified to be *at least* 50.



(a)



(b)

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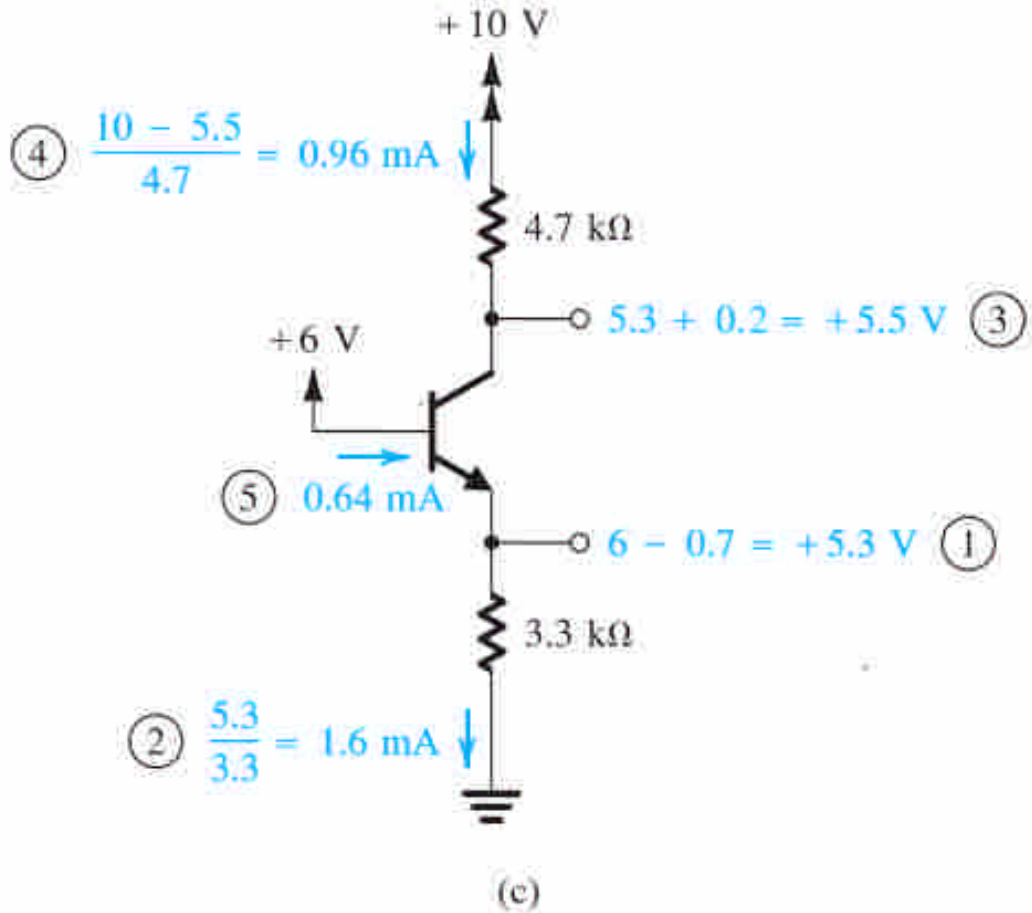

(c)

FIGURE 5.35 Analysis of the circuit for Example 5.5. Note that the circled numbers indicate the order of the analysis steps.

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Solution

Assuming active-mode operation, we have

$$V_E = +6 - V_{BE} \simeq 6 - 0.7 = 5.3 \text{ V}$$

$$I_E = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

$$V_C = +10 - 4.7 \times I_C \simeq 10 - 7.52 = 2.48 \text{ V}$$

The details of the analysis performed above are illustrated in Fig. 5.35(b).

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Since the collector voltage calculated appears to be less than the base voltage by 3.52 V, it follows that our original assumption of active-mode operation is incorrect. In fact, the transistor has to be in the *saturation* mode. Assuming this to be the case, we have

$$V_E = +6 - 0.7 = +5.3 \text{ V}$$

$$I_E = \frac{V_E}{3.3} = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

$$V_C = V_E + V_{CE\text{sat}} \simeq +5.3 + 0.2 = +5.5 \text{ V}$$

$$I_C = \frac{+10 - 5.5}{4.7} = 0.96 \text{ mA}$$

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA}$$

Thus the transistor is operating at a forced β of

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

Since β_{forced} is less than the *minimum* specified value of β, the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of β should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified β. Obviously, if a transistor with this minimum β is saturated, then transistors with higher values of β will also be saturated. The details of the analysis are shown in Fig. 5.35(c), where the order of the steps used is indicated by the circled numbers.

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EXAMPLE 5.6

We wish to analyze the circuit in Fig. 5.36(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that considered in Examples 5.4 and 5.5 except that now the base voltage is zero.

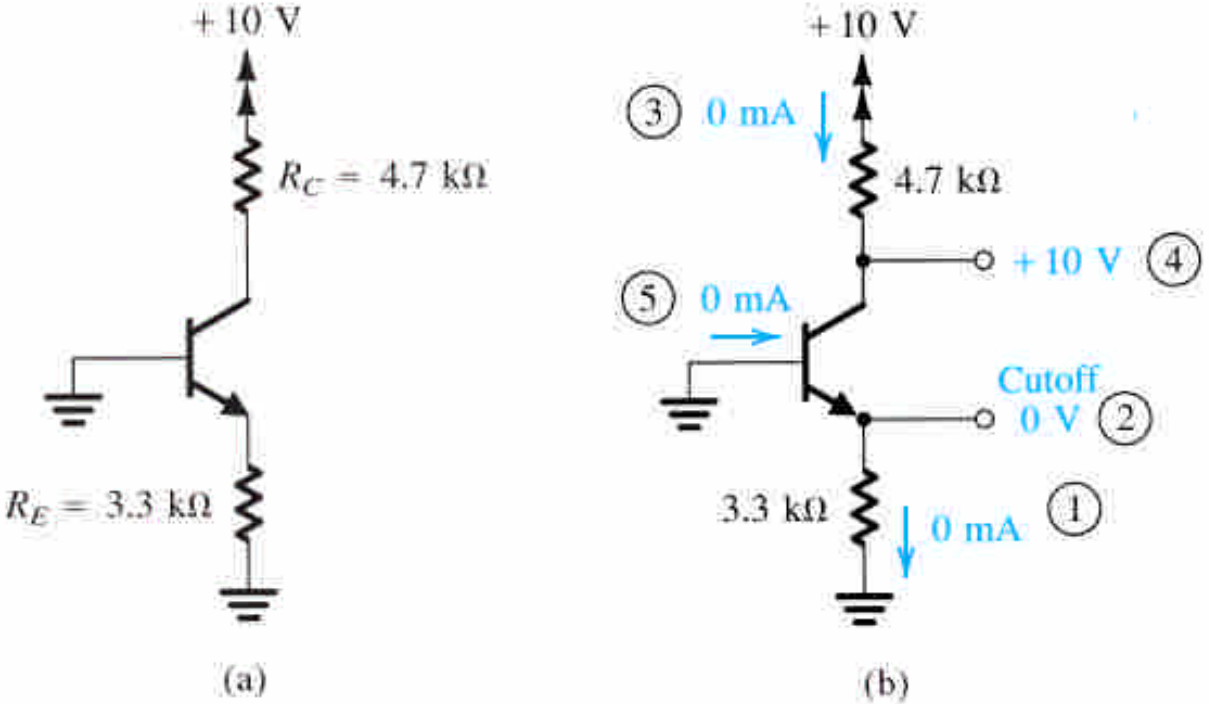

FIGURE 5.36 Example 5.6: (a) circuit; (b) analysis with the order of the analysis steps indicated by circled numbers.

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Solution

Since the base is at zero volts, the emitter–base junction cannot conduct and the emitter current is zero. Also, the collector–base junction cannot conduct since the *n*-type collector is connected through R_C to the positive power supply while the *p*-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the *cutoff* mode of operation.

The emitter voltage will obviously be zero, while the collector voltage will be equal to +10 V, since the voltage drop across R_C is zero. Figure 5.36(b) shows the analysis details.

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5.5 BIASING IN BJT AMPLIFIER CIRCUITS

- The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculable, predictable, and insensitive to variations in temperature and to the large variations in the value of β encountered among transistors of the same type.

5.5.1 Classical Discrete-Circuit Bias Arrangement

- Figure 5.44(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available.

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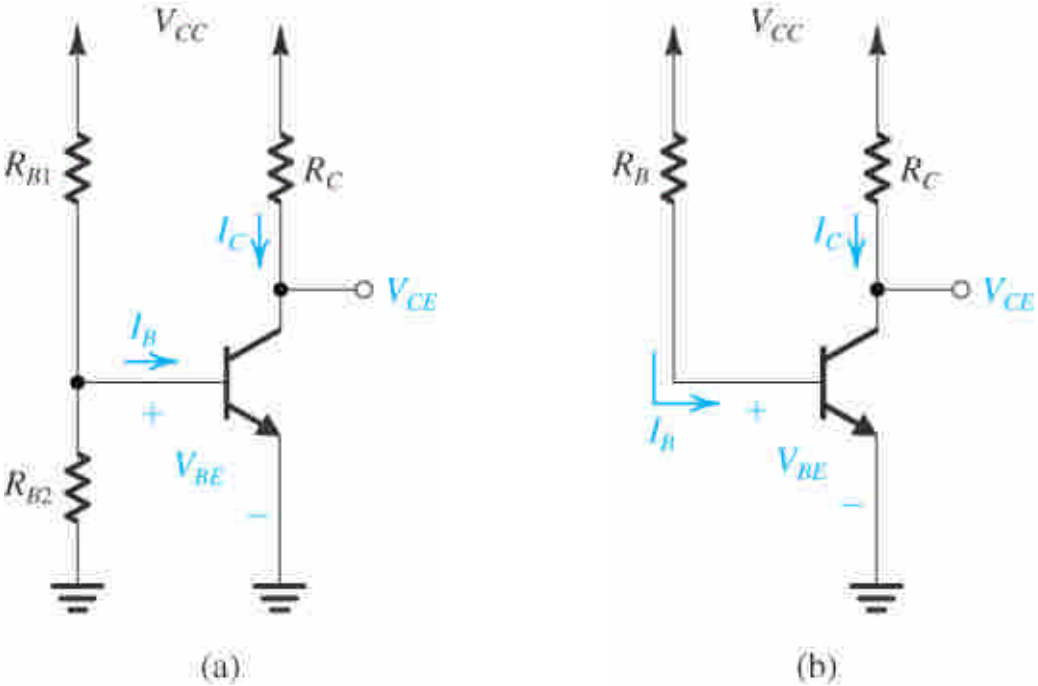

Figure 5.43 Two obvious schemes for biasing the BJT: **(a)** by fixing V_{BE}; **(b)** by fixing I_B. Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be "bad." Neither scheme is recommended.

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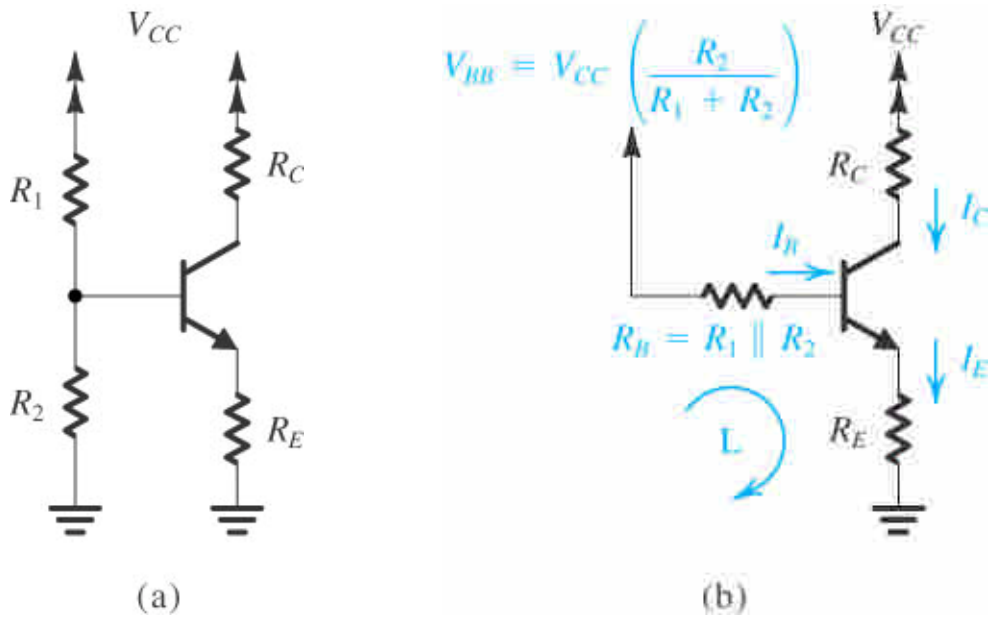

Figure 5.44 Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

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$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{5.68}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{5.69}$$

substituting $I_B = I_E/(\beta + 1)$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{5.70}$$

- To make *IE* insensitive to temperature and β variation, we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE} \tag{5.71}$$

$$R_E \gg \frac{R_B}{\beta + 1} \tag{5.72}$$

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- As a rule of thumb, one designs for

V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC}$, and $I_C R_C$ about $\frac{1}{3}V_{CC}$.

- Typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$.

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EXAMPLE 5.13

We wish to design the bias network of the amplifier in Fig. 5.44 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.

Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across R_2 and another one-third to the voltage drop across R_C, leaving one-third for possible signal swing at the collector. Thus,

$$V_B = +4 \text{ V}$$

$$V_E = 4 - V_{BE} \simeq 3.3 \text{ V}$$

and R_E is determined from

$$R_E = \frac{V_E}{I_E} = 3.3 \text{ k}\Omega$$

From the discussion above we select a voltage-divider current of $0.1I_E = 0.1 \times 1 = 0.1$ mA. Neglecting the base current, we find

$$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

and

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

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Thus $R_2 = 40\ \text{k}\Omega$ and $R_1 = 80\ \text{k}\Omega$.

At this point, it is desirable to find a more accurate estimate for I_E, taking into account the nonzero base current. Using Eq. (5.70),

$$I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \dfrac{(80 \,/\!/\, 40)(\text{k}\Omega)}{101}} = 0.93\ \text{mA}$$

This is quite a bit lower than the value we are aiming for of 1 mA. It is easy to see from the above equation that a simple way to restore I_E to its nominal value would be to reduce R_E from 3.3 kΩ by the magnitude of the second term in the denominator (0.267 kΩ). Thus a more suitable value for R_E in this case would be $R_E = 3\ \text{k}\Omega$, which results in $I_E = 1.01\ \text{mA} \simeq 1\ \text{mA}$.

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to I_E (i.e., 1 mA), resulting in $R_1 = 8\ \text{k}\Omega$ and $R_2 = 4\ \text{k}\Omega$. We shall refer to the circuit using these latter values as design 2, for which the actual value of I_E using the initial value of R_E of 3.3 kΩ will be

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1\ \text{mA}$$

In this case, design 2, we need not change the value of R_E.

Finally, the value of R_C can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99\ \text{mA} \simeq 1\ \text{mA}$ results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4\ \text{k}\Omega$$

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5.5.2 A Two Power-Supply Version of the Classical Bias Arrangement

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)} \qquad (5.73)$$

This equation is identical to Eq. (5.70) except for V_{EE} replacing V_{BB}. Thus the two con- straints of Eqs. (5.71) and (5.72) apply here as well.

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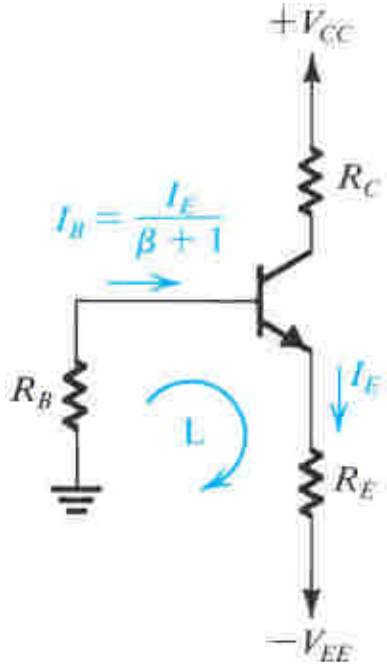

Figure 5.45 Biasing the BJT using two power supplies. Resistor R_B is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β-independence of the bias current.

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5.5.3 Biasing Using a Collector-to-Base Feedback Resistor

$$V_{CC} = I_E R_C + I_B R_B + V_{BE}$$

$$= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE}$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)} \qquad (5.74)$$

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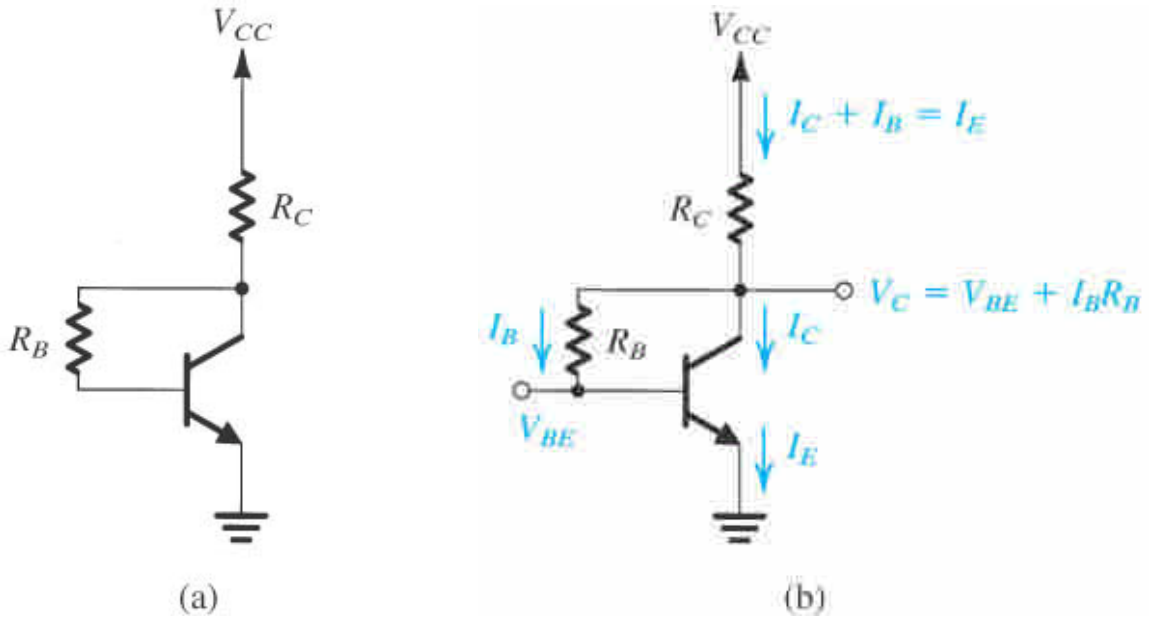

Figure 5.46 (a) A common-emitter transistor amplifier biased by a feedback resistor R_B. **(b)** Analysis of the circuit in (a).

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5.6 SMALL-SIGNAL OPERATION AND MODELS

- We consider first the dc bias conditions by setting the signal v_{be} to zero. The circuit reduces to that in Fig. 5.48(b), and we can write the following relationships for the dc currents and voltages:

$$I_C = I_S e^{V_{BE}/V_T} \quad (5.78)$$

$$I_E = I_C/\alpha \quad (5.79)$$

$$I_B = I_C/\beta \quad (5.80)$$

$$V_C = V_{CE} = V_{CC} - I_C R_C \quad (5.81)$$

- Obviously, for active-mode operation, V_C should be greater than $(V_B - 0.4)$

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5.6.1 The Collector Current and the Transconductance

the total instantaneous base–emitter voltage v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$

$$= I_S e^{(V_{BE}/V_T)} e^{(v_{be}/V_T)}$$

$$i_C = I_C e^{v_{be}/V_T} \tag{5.82}$$

Now, if $v_{be} \ll V_T$, we may approximate Eq. (5.82) as

$$i_C \simeq I_C\left(1 + \frac{v_{be}}{V_T}\right) \tag{5.83}$$

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- This approximation, which is valid only for v_{be} less than approximately 10 mV, is referred to as the **small-signal approximation.**

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \tag{5.84}$$

Thus the collector current is composed of the dc bias value I_C and a signal component i_c,

$$i_c = \frac{I_C}{V_T} v_{be} \tag{5.85}$$

$$i_c = g_m v_{be} \tag{5.86}$$

where g_m is called the **transconductance,**

$$g_m = \frac{I_C}{V_T} \tag{5.87}$$

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- The small-signal approximation implies keeping the signal amplitude sufficiently small so that *operation is restricted to an almost-linear segment of the i_C–v_{BE} exponential curve.*

- The analysis above suggests that for small signals ($v_{be} << V_T$), the transistor behaves as a voltage-controlled current source.

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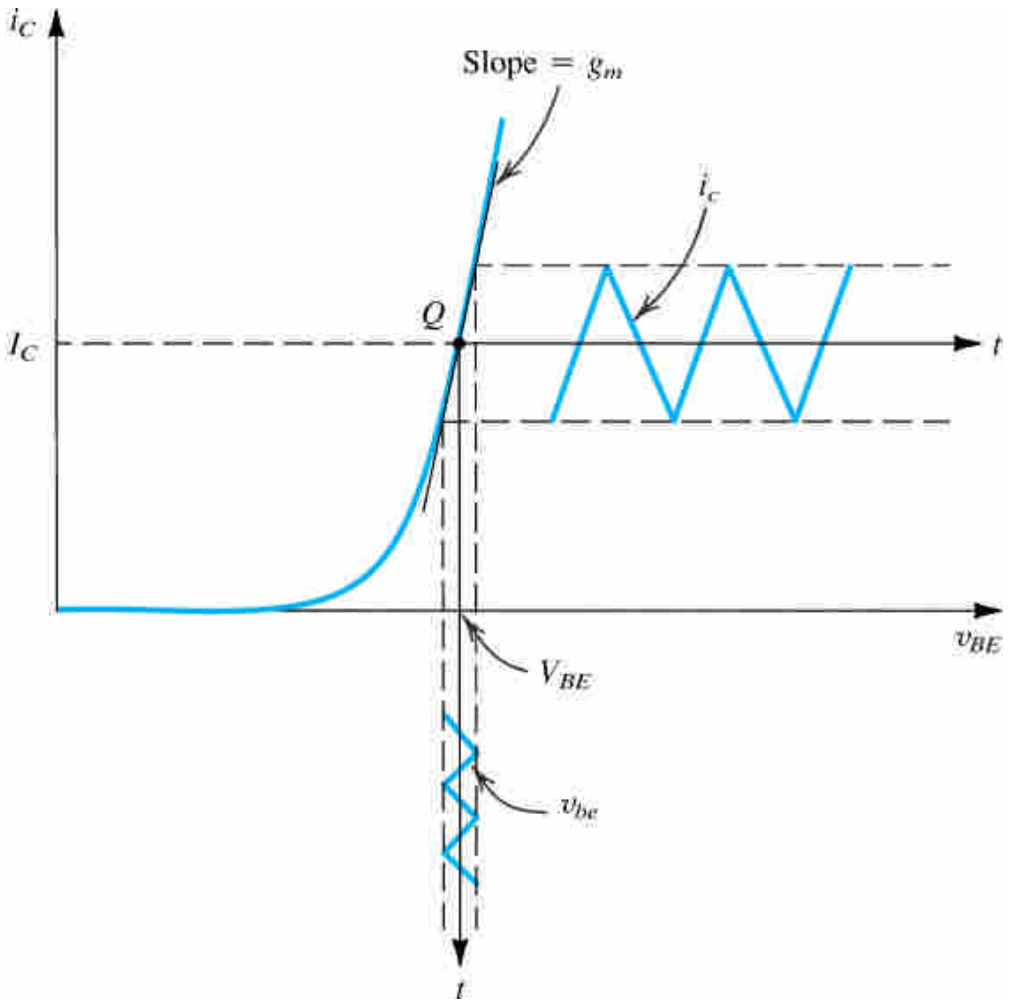

Figure 5.49 Linear operation of the transistor under the small-signal condition: A small signal v_{be} with a triangular waveform is superimposed on the dc voltage V_{BE}. It gives rise to a collector signal current i_c, also of triangular waveform, superimposed on the dc current I_C. Here, $i_c = g_m v_{be}$, where g_m is the slope of the i_C–v_{BE} curve at the bias point Q.

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5.6.2 The Base Current and the Input Resistance at the Base

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

$$i_B = I_B + i_b \tag{5.89}$$

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be} \tag{5.90}$$

Substituting for I_C/V_T by g_m gives

$$i_b = \frac{g_m}{\beta}v_{be} \tag{5.91}$$

$$r_\pi \equiv \frac{v_{be}}{i_b} \tag{5.92}$$

$$r_\pi = \frac{\beta}{g_m} \tag{5.93}$$

$$r_\pi = \frac{V_T}{I_B} \tag{5.94}$$

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5.6.3 The Emitter Current and the Input Resistance at the Emitter

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

$$i_E = I_E + i_e \qquad (5.95)$$

- If we denote the small-signal resistance between base and emitter, *looking into the emitter*,by r_e, it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e} \qquad (5.97) \qquad r_e = \frac{V_T}{I_E} \qquad (5.98)$$

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m} \qquad (5.99)$$

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- The relationship between r_π and r_e can be found by combining their respective definitions in Eqs. (5.92) and (5.97) as

$$v_{be} = i_b r_\pi = i_e r_e$$

$$r_\pi = (i_e / i_b) r_e$$

$$r_\pi = (\beta + 1) r_e \qquad (5.100)$$

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5.6.4 Voltage Gain

$$A_v \equiv \frac{v_c}{v_{be}} = -g_m R_C \qquad (5.103)$$

5.6.6 The Hybrid- π Model

An equivalent circuit model for the BJT is shown in Fig. 5.51(a).

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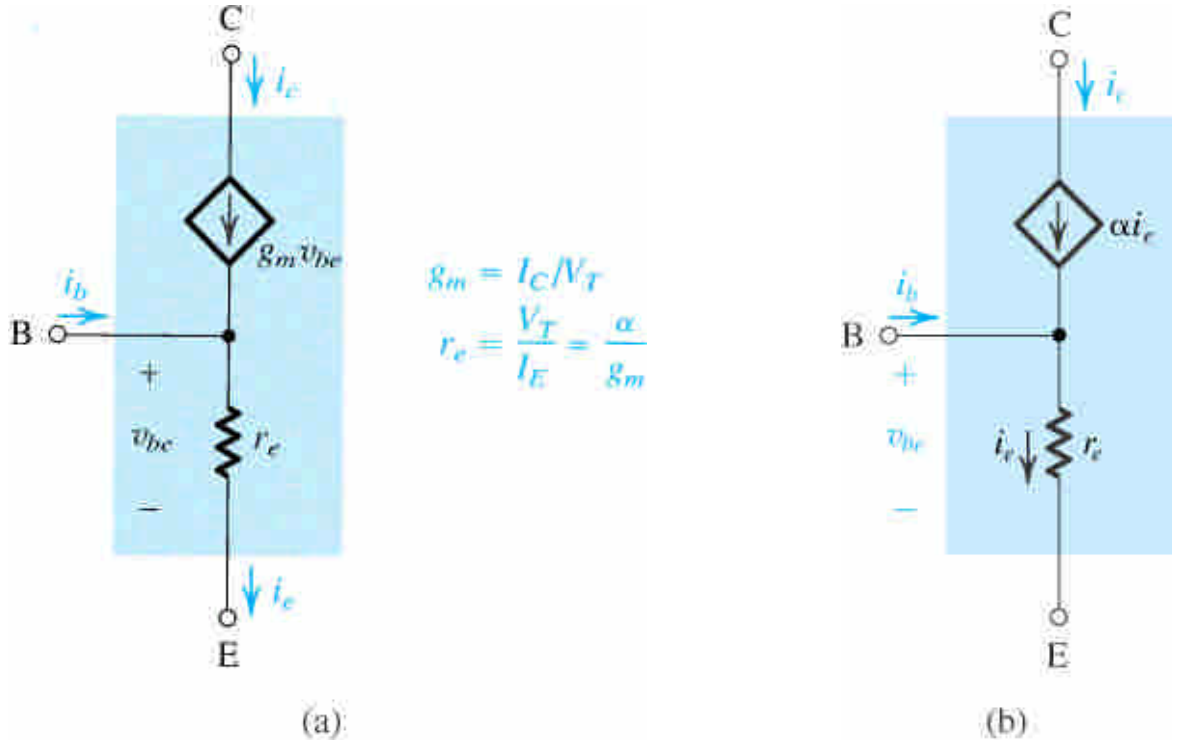

Figure 5.52 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in **(a)** is a voltage-controlled current source representation and that in **(b)** is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid-π model.

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The model obviously yields $i_c = g_m v_{be}$ and $i_b = v_{be} / r_\pi$.

$$
\begin{aligned}
i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi) \\
&= \frac{v_{be}}{r_\pi}(1 + \beta) = v_{be} \Big/ \left(\frac{r_\pi}{1+\beta}\right) \\
&= v_{be} / r_e \\
g_m v_{be} &= g_m (i_b r_\pi) \\
&= (g_m r_\pi) i_b = \beta i_b
\end{aligned}
$$

- The two models of Fig. 5.51 are simplified versions of what is known as the hybrid- π model. This is the most widely used model for the BJT.

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5.6.7 The T Model

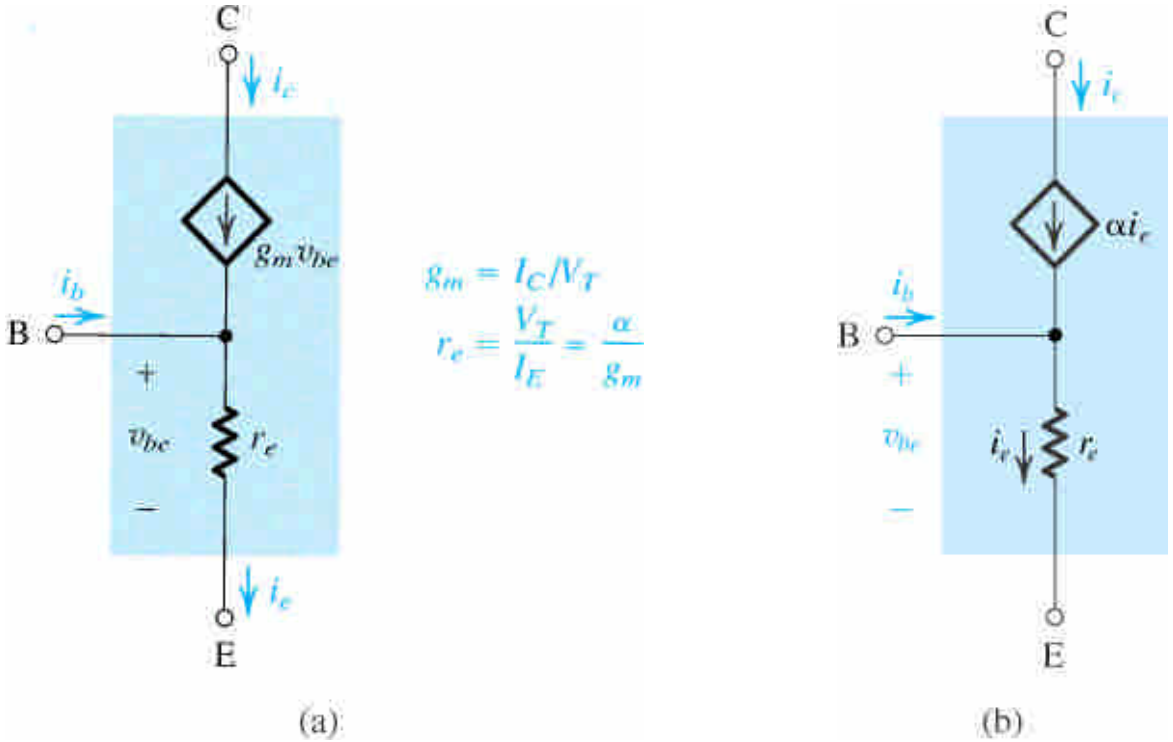

Figure 5.52 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in **(a)** is a voltage-controlled current source representation and that in **(b)** is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid-π model.

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5.6.8 Application of the Small-Signal Equivalent Circuits

The process consists of the following steps:

1. Determine the dc operating point of the BJT and in particular the dc collector current *IC*.
2. Calculate the values of the small-signal model parameters: $g_m = I_C / V_T$, $r_\pi = \beta / g_m$ $r_e = V_T / I_E \cong 1 / g_m$
3. Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
4. Replace the BJT with one of its small-signal equivalent circuit models.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance). The process will be illustrated by the following examples.

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EXAMPLE 5.14

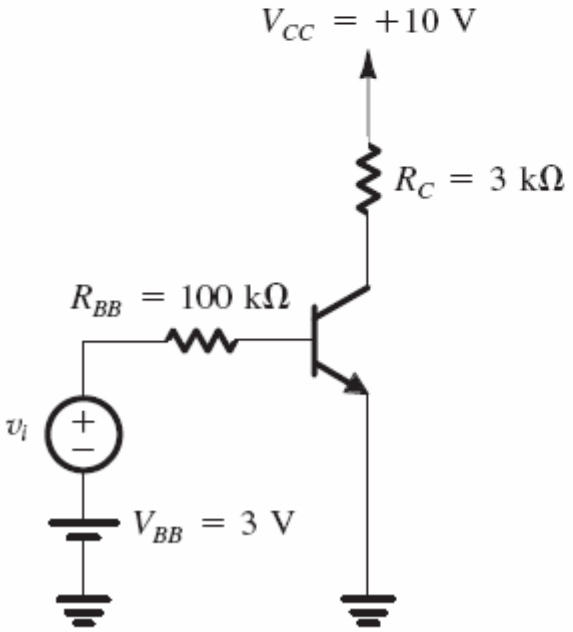
We wish to analyze the transistor amplifier shown in Fig. 5.53(a) to determine its voltage gain. Assume $\beta = 100$.

Solution

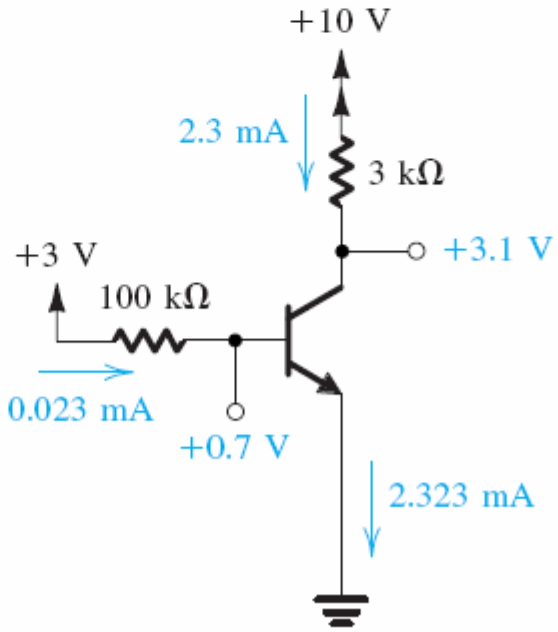
The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $v_i = 0$. The dc base current will be

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}}$$

$$\simeq \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$



(a)



(b)

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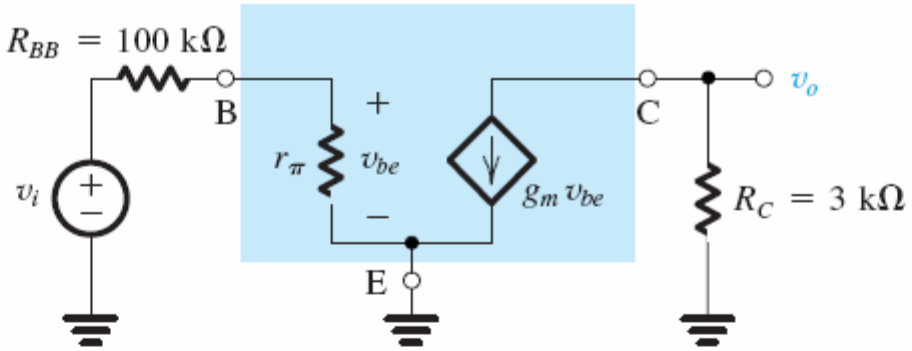

(c)

FIGURE 5.53 Example 5.14: **(a)** circuit; **(b)** dc analysis; **(c)** small-signal model.

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$V_C = V_{CC} - I_C R_C$$
$$= +10 - 2.3 \times 3 = +3.1 \text{ V}$$

Since V_B at +0.7 V is less than V_C, it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 5.53(b).

Having determined the operating point, we may now proceed to determine the small-signal model parameters:

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3/0.99) \text{ mA}} = 10.8 \ \Omega$$

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$$g_m = \frac{I_C}{V_T} = \frac{2.3\text{ mA}}{25\text{ mV}} = 92\text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09\text{ k}\Omega$$

To carry out the small-signal analysis it is equally convenient to employ either of the two hybrid-π equivalent circuit models of Fig. 5.51. Using the first results in the amplifier equivalent circuit given in Fig. 5.53(c). Note that no dc quantities are included in this equivalent circuit. It is most important to note that the dc supply voltage V_{CC} has been replaced by a *short circuit* in the signal equivalent circuit because the circuit terminal connected to V_{CC} will always have a constant voltage. That is, the signal voltage at this terminal will be zero. In other words, *a circuit terminal connected to a constant dc source can always be considered as a signal ground.*

Analysis of the equivalent circuit in Fig. 5.53(c) proceeds as follows:

$$\begin{aligned} v_{be} &= v_i \frac{r_\pi}{r_\pi + R_{BB}} \\ &= v_i \frac{1.09}{101.09} = 0.011 v_i \end{aligned} \tag{5.105}$$

The output voltage v_o is given by

$$\begin{aligned} v_o &= -g_m v_{be} R_C \\ &= -92 \times 0.011 v_i \times 3 = -3.04 v_i \end{aligned}$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04\text{ V/V} \tag{5.106}$$

where the minus sign indicates a phase reversal.

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5.6.10 Augmenting the Small-Signal Models to Accountfor the Early Effect

- The Early effect, discussed in Section 5.2, causes the collector current to depend not only on v_{BE} but also on v_{CE}. The dependence on v_{CE} can be modeled by assigning a finite output resistance to the controlled current-source in the hybrid-π model, as shown in Fig. 5.58. The output resistance r_o was defined in Eq. (5.37); its value is given by

$$r_o = (V_A + V_{CE}) / I_C \cong I_C$$

the output voltage v_o becomes $v_o = -g_m v_{be}(R_C // r_o)$

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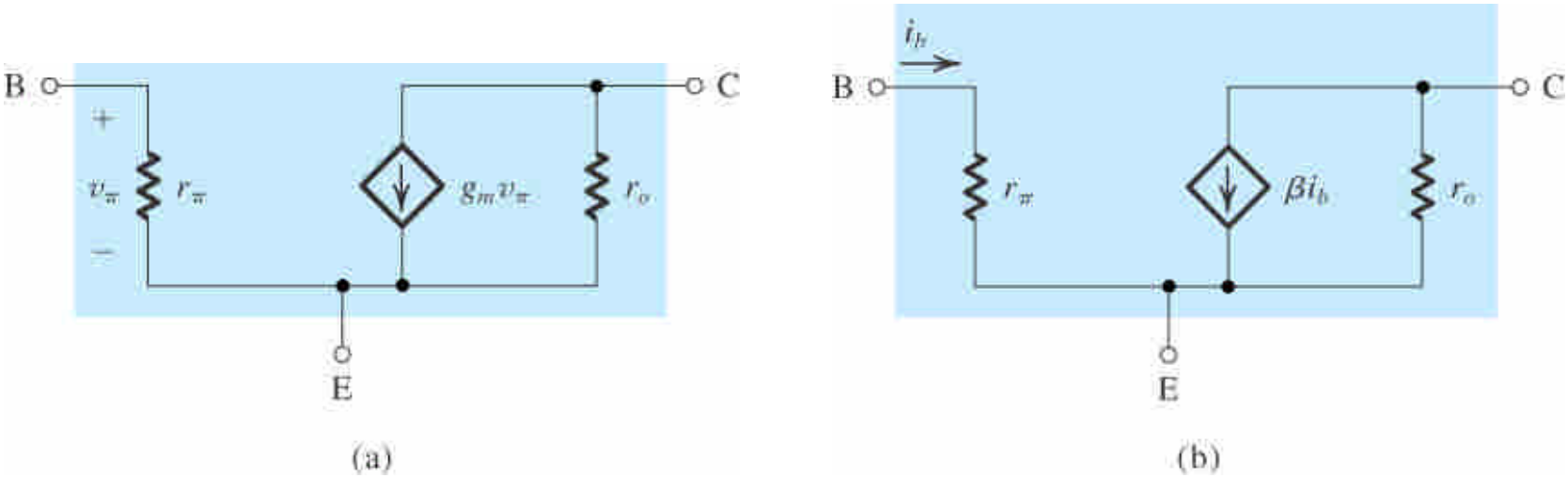

Figure 5.58 The hybrid-π small-signal model, in its two versions, with the resistance r_o included.

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5.7 SINGLE-STAGE BJT AMPLIFIERS

There are basically three configurations for implementing single-stage BJT amplifiers: the common-emitter, the common-base, and the common-collector configurations.

5.7.1 The Basic Structure

Figure 5.59 shows the basic circuit

5.7.2 Characterizing BJT Amplifiers

Table 5.5

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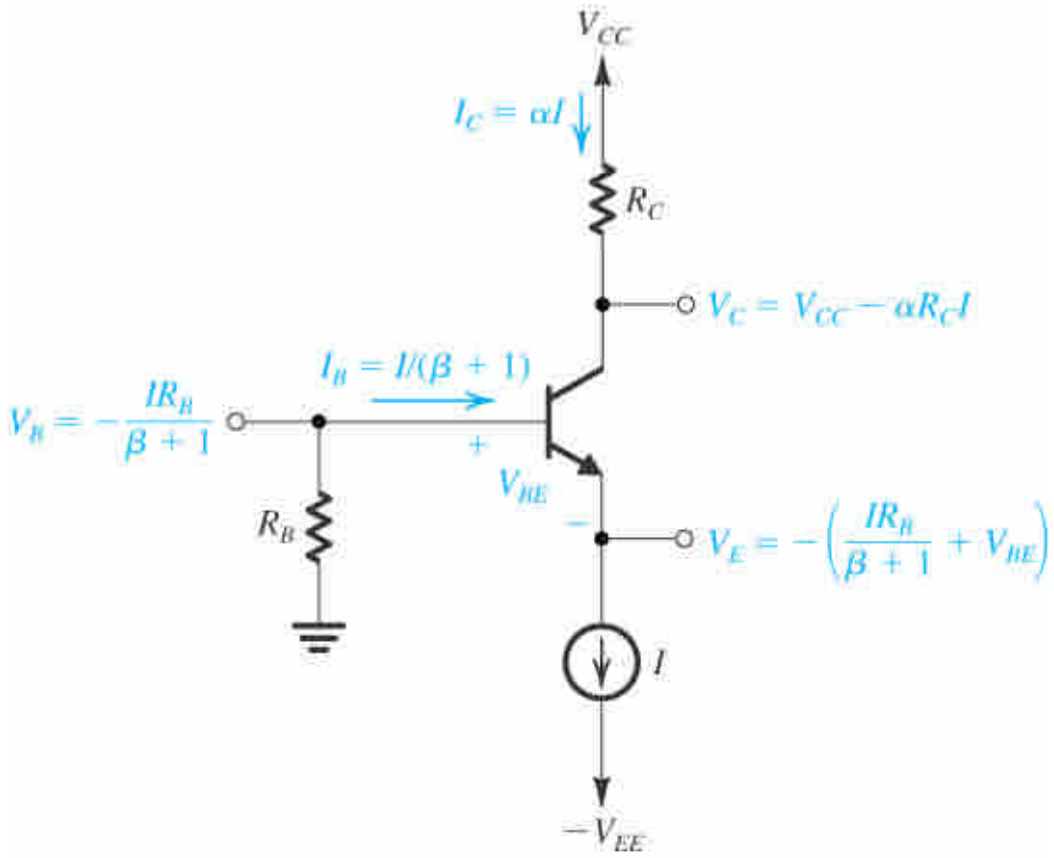

Figure 5.59 Basic structure of the circuit used to realize single-stage, discrete-circuit BJT amplifier configurations.

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5.7.3 The Common-Emitter Amplifier

- The CE configuration is the most widely used of all BJT amplifier circuits. Figure 5.60(a) shows a CE amplifier implemented using the circuit of Fig. 5.59.

- A large capacitor *CE*, usually in the μF or tens of μF range, is connected between emitter and ground. This capacitor is required to provide a very low impedance to ground.

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- In this way, the emitter signal current passes through C_E to ground and thus *bypasses* the output resistance of the current source *I*

C_E is called a **bypass capacitor.**

- Here we shall assume that C_E is acting as a perfect short circuit and thus is establishing a zero signal voltage at the emitter.

- Capacitor C_{C1}, known as a **coupling capacitor,** is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc.

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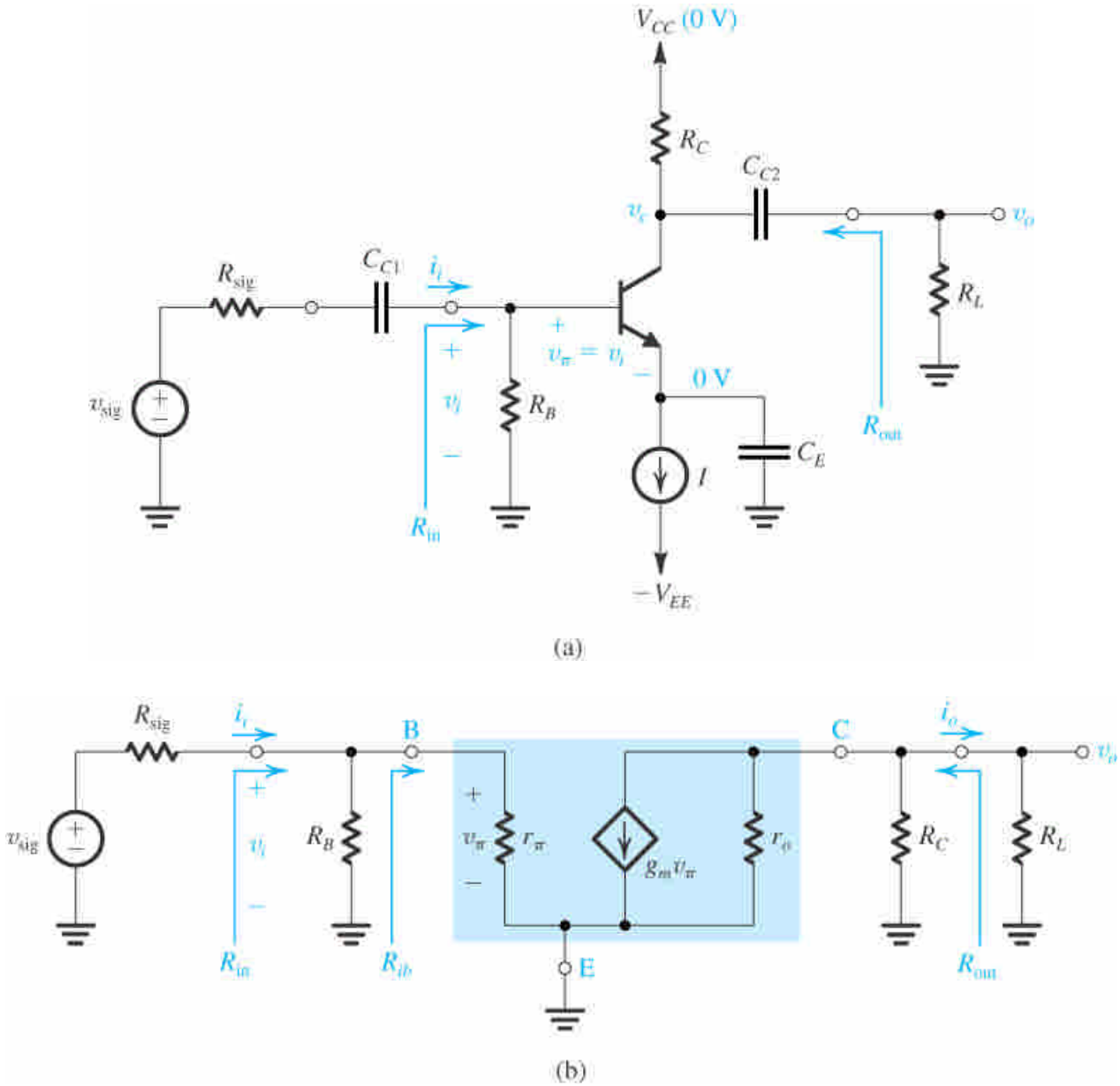

Figure 5.60 **(a)** A common-emitter amplifier using the structure of Fig. 5.59. **(b)** Equivalent circuit obtained by replacing the transistor with its hybrid-π model.

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- The voltage signal resulting at the collector, *vc*, is coupled to the load resistance R_L via another coupling capacitor C_{C2}. We shall assume that C_{C2} also acts a perfect short circuit at all signal frequencies of interest; thus the output voltage $v_o = v_c$.
- To determine the terminal characteristics of the CE amplifier, that is, its input resistance, voltage gain, and output resistance, we replace the BJT with its hybrid-π small-signal model.

Thus $R_{\text{in}} = R_i$ and $R_{\text{out}} = R_o$

$$R_{\text{in}} \equiv \frac{v_i}{i_i} = R_B \parallel R_{ib} \qquad (5.109) \qquad R_{ib} = r_\pi \qquad (5.110)$$

Normally, we select $R_B \gg r_\pi$, with the result that

$$R_{\text{in}} \cong r_\pi \qquad (5.111)$$

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$$v_i = v_{\text{sig}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \qquad (5.112)$$

$$= v_{\text{sig}} \frac{(R_B \parallel r_\pi)}{(R_B + r_\pi) + R_{\text{sig}}} \qquad (5.113)$$

which for $R_B \gg r_\pi$ becomes

$$v_i \cong v_{\text{sig}} \frac{r_\pi}{r_\pi + R_{\text{sig}}} \qquad (5.114) \qquad v_\pi = v_i \qquad (5.115)$$

At the output of the amplifier we have

$$v_o = -g_m v_\pi (r_o \parallel R_C \parallel R_L)$$

$$A_v = -g_m (r_o \parallel R_C \parallel R_L) \qquad (5.116)$$

The open-circuit voltage gain A_{vo} can be obtained by setting $R_L = \infty$ in Eq. (5.116); thus,

$$A_{vo} = -g_m (r_o \parallel R_C) \qquad (5.117)$$

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since typically $r_o \gg R_C$, resulting in

$$A_{vo} \cong -g_m R_C \tag{5.118}$$

$$R_{\text{out}} = R_C \parallel r_o \tag{5.119}$$

$$R_{\text{out}} \cong R_C \tag{5.120}$$

The overall voltage gain from source to load, G_v, can be obtained by multiplying (v_i / v_{sig}) from Eq. (5.114) by A_v from Eq. (5.116),

$$G_v = -\frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m (r_o \parallel R_C \parallel R_L) \tag{5.121}$$

if $R_s \ll r_\pi$, we see that the expression for the overall voltage gain reduces to

$$G_v \cong -g_m (R_C \parallel R_L \parallel r_o) \tag{5.123}$$

which is the gain A_V; in other words, when R_s is small, the overall voltage gain is almost equal to the gain of the CE circuit proper, which is independent of β.

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- It follows that the CE amplifier is used to realize the bulk of the voltage gain required in a unusual amplifier design
- we wish to evaluate its short-circuit current gain, A_{is}. This can be easily done by referring to the amplifier equivalent circuit in Fig. 5.60(b). When R_L is short circuited, the current through it will be equal to $-g_m v_\pi$,

$$i_{os} = -g_m v_\pi$$

$$v_\pi = v_i = i_i R_{\text{in}}$$

$$A_{is} \equiv \frac{i_{os}}{i_i} = -g_m R_{\text{in}} \qquad (5.124)$$

- In conclusion, the common-emitter configuration can provide large voltage and current gains, but R_{in} is relatively low and R_{out} is relatively high.

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5.7.4 The Common-Emitter Amplifier with an Emitter Resistance

$$R_{\text{in}} = R_B \parallel R_{ib} \tag{5.125}$$

$$R_{ib} \equiv \frac{v_i}{i_b} \qquad i_b = (1-\alpha)i_e = \frac{i_e}{\beta+1}$$

$$i_e = \frac{v_i}{r_e + R_e} \tag{5.126}$$

$$R_{ib} = (\beta+1)(r_e + R_e) \tag{5.127}$$

the input resistance looking into the base is (β+1) times the total resistance in the emitter. Multiplication by the factor (β+1) is known as the **resistance-reflection rule.**

$$\frac{R_{ib}\,(\text{with } R_e \text{ included})}{R_{ib}\,(\text{without } R_e)} = \frac{(\beta+1)(r_e+R_e)}{(\beta+1)r_e} = 1 + \frac{R_e}{r_e} \cong 1 + g_m R_e \tag{5.128}$$

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- Thus the circuit designer can use the value of *Re* to control the value of R_{ib} and hence R_{in}.
- To determine the voltage gain A_v,

$$v_o = -i_c(R_C \parallel R_L) = -\alpha i_e(R_C \parallel R_L)$$

Substituting for *ie* from Eq. (5.126) gives

$$A_v \equiv \frac{v_o}{v_i} = -\frac{\alpha(R_C \parallel R_L)}{r_e + R_e} \qquad (5.129)$$

$$\text{Since } \alpha \cong 1, \qquad A_v \cong -\frac{R_C \parallel R_L}{r_e + R_e} \qquad (5.130)$$

- *The voltage gain from base to collector is equal to the ratio of the total resistance in the collector to the total resistance in the emitter*.

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- The open-circuit voltage gain *Avo* can be found by setting $RL = \infty$ in Eq. (5.129),

$$A_{vo} = -\frac{\alpha R_C}{r_e + R_e} \qquad (5.131)$$

- The short-circuit current gain A_{is} can be found from the circuit in Fig. 5.61(b) as follows:

$$i_{os} = -\alpha i_e \qquad i_i = v_i / R_{\text{in}} \qquad A_{is} = -\frac{\alpha R_{\text{in}} i_e}{v_i}$$

$$A_{is} = -\frac{\alpha (R_B \parallel R_{ib})}{r_e + R_e} \qquad (5.134)$$

$$A_{is} = \frac{-\alpha(\beta + 1)(r_e + R_e)}{r_e + R_e} = -\beta$$

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- The overall voltage gain from source to load can be obtained by multiplying *Av* by (v_i/v_{sig})

$$G_v = \frac{v_i}{v_s} \cdot A_v = -\frac{R_{in}}{R_{sig} + R_{in}} \frac{\alpha(R_B \parallel R_{ib})}{r_e + R_e}$$

Substituting for R_i by $R_B \parallel R_{ib}$, assuming that $R_B \gg R_{ib}$, and substituting for R_{ib} from Eq. (5.127) results in

$$G_v = -\frac{\beta(R_C \parallel R_L)}{R_{sig} + (\beta + 1)(r_e + R_e)} \qquad (5.135)$$

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- Another important consequence of including the resistance R_e in the emitter is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion.

- Finally, we note that the negative feedback action of R_e gives it the name **emitter degeneration resistance.**

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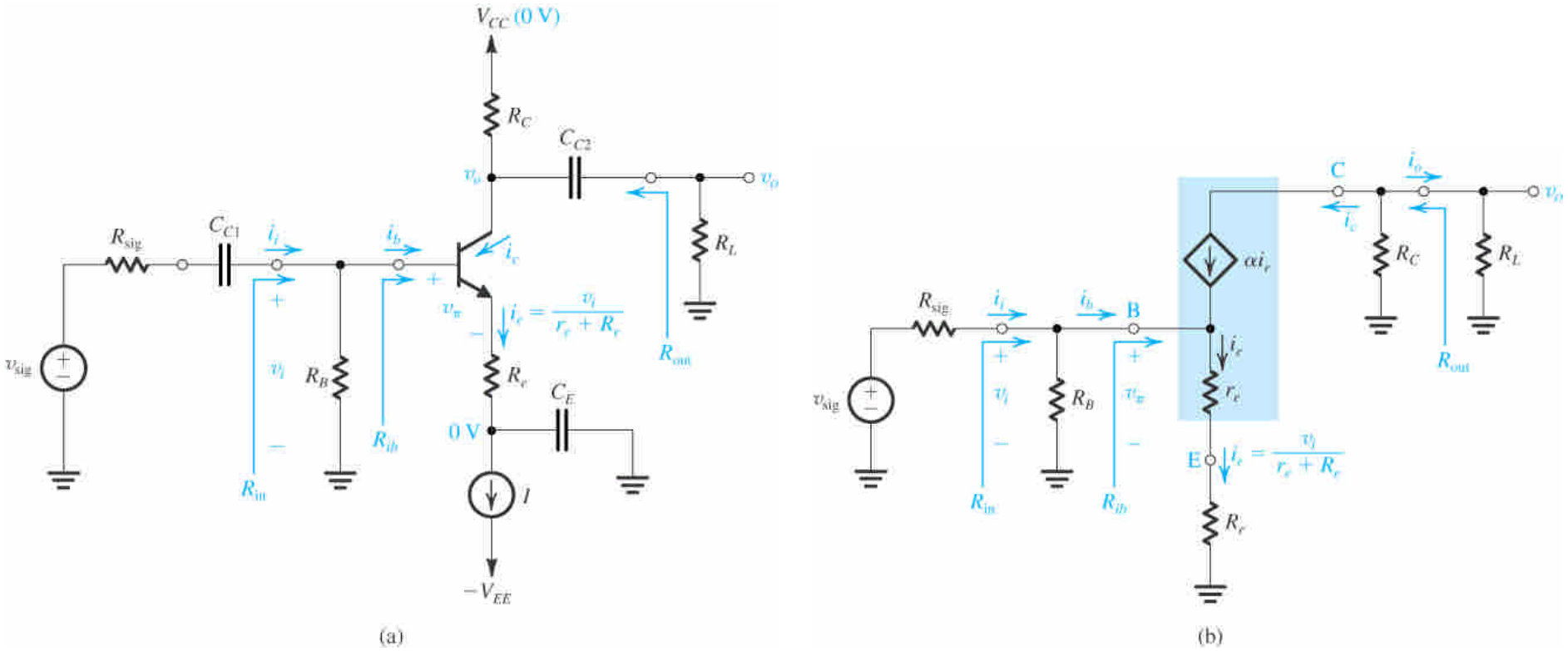

Figure 5.61 **(a)** A common-emitter amplifier with an emitter resistance R_e. **(b)** Equivalent circuit obtained by replacing the transistor with its T model.

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5.7.5 The Common-Base Amplifier

- By establishing a signal ground on the base terminal of the BJT, a circuit configuration aptly named common-base or **grounded-base amplifier** is obtained.

$$R_{in} = r_e \qquad (5.137)$$

thus the CB amplifier has a low input resistance.

- To determine the voltage gain,

$$v_o = -\alpha i_e (R_C \parallel R_L) \qquad i_e = -\frac{v_i}{r_e}$$

$$A_v \equiv \frac{v_o}{v_i} = \frac{\alpha}{r_e}(R_C \parallel R_L) = g_m (R_C \parallel R_L) \qquad (5.138)$$

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- The open-circuit voltage gain A_{vo} can be found from Eq. (5.138) by setting $R_L = \infty$:

$$A_{vo} = g_m R_C \tag{5.139}$$

$$R_{\text{out}} = R_C$$

- The short-circuit current gain A_{is} is given by

$$A_{is} = \frac{-\alpha i_e}{i_i} = \frac{-\alpha i_e}{-i_e} = \alpha \tag{5.140}$$

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_i}{R_{\text{sig}} + R_i} = \frac{r_e}{R_{\text{sig}} + r_e} \tag{5.141}$$

$$G_v = \frac{r_e}{R_{\text{sig}} + r_e} g_m (R_C \parallel R_L) = \frac{\alpha (R_C \parallel R_L)}{R_{\text{sig}} + r_e} \tag{5.142}$$

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- In summary, the CB amplifier exhibits a very low input resistance (r_e) a short-circuit current gain that is nearly unity (α), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE amplifier ($g_m R_C$), and like the CE amplifier, a relatively high output resistance (R_C).

- Finally, a very significant application of the CB circuit is as a unity-gain current amplifier or **current buffer:** It accepts an input signal current at a low input resistance and delivers a nearly equal current at very high output resistance at the collector

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5.7.6 The Common-Collector (CC) Amplifier or Emitter Follower

$$R_{ib} = (\beta + 1)[r_e + (r_o \parallel R_L)] \tag{5.143}$$

$$R_{\text{in}} = R_B \parallel R_{ib}$$

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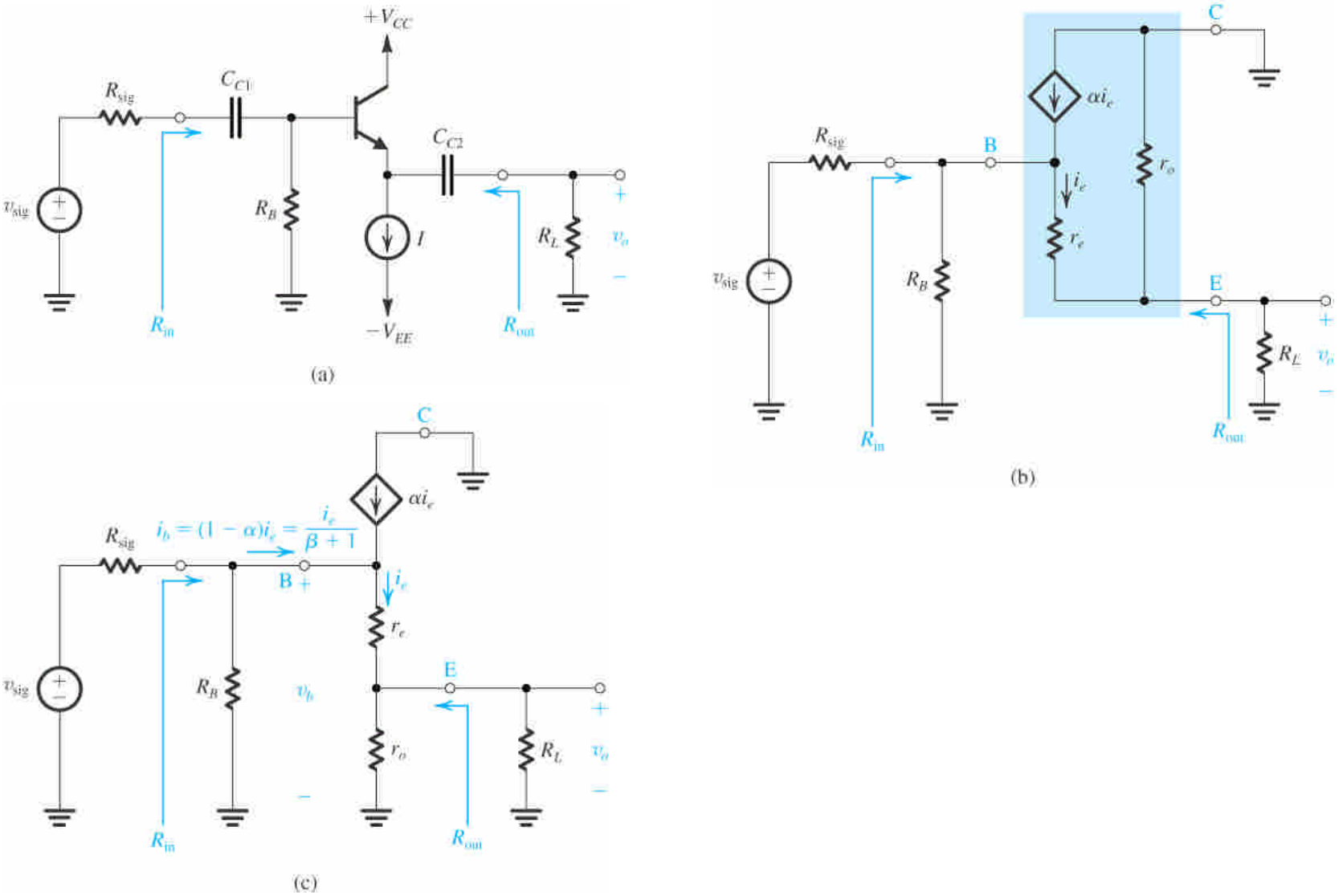

Figure 5.63 **(a)** An emitter-follower circuit based on the structure of Fig. 5.59. **(b)** Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model augmented with r_o. **(c)** The circuit in (b) redrawn to emphasize that r_o is in parallel with R_L. This simplifies the analysis considerably.

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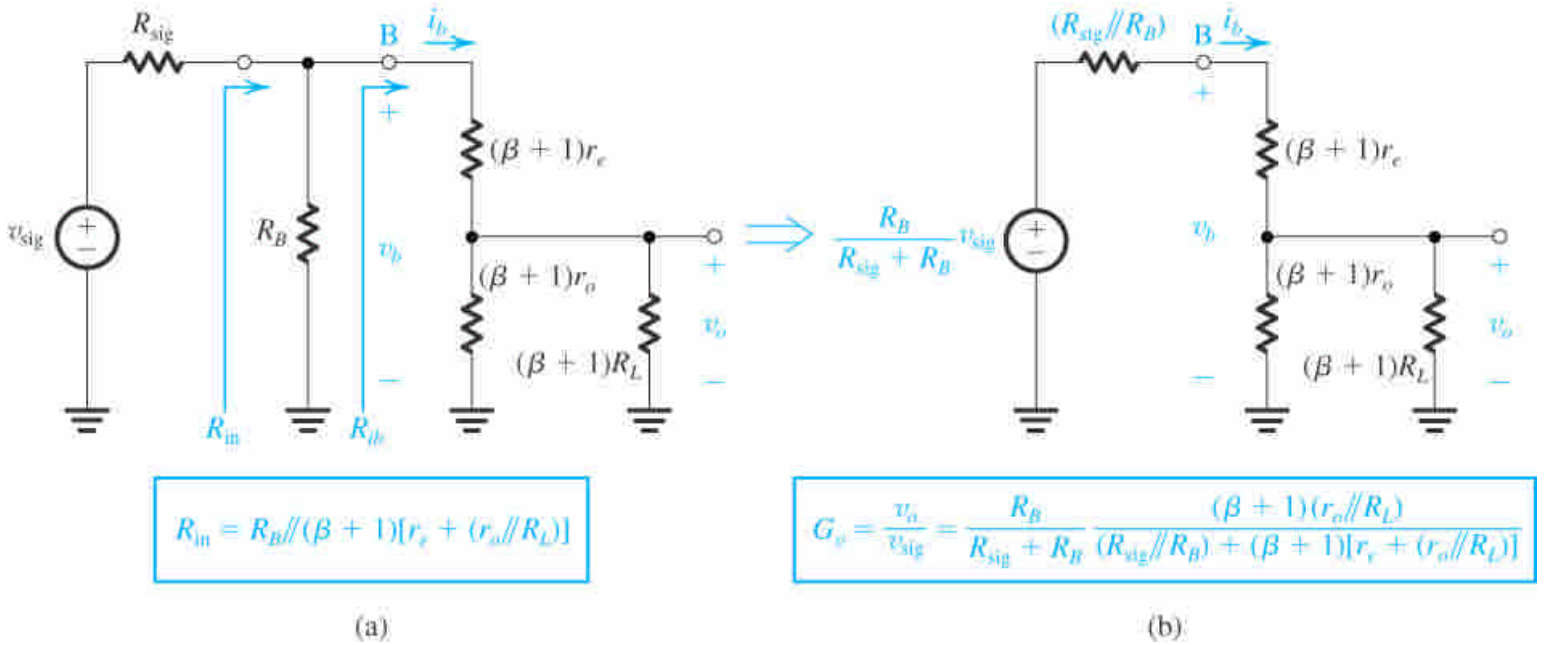

Figure 5.64 **(a)** An equivalent circuit of the emitter follower obtained from the circuit in Fig. 5.63(c) by reflecting all resistances in the emitter to the base side. **(b)** The circuit in (a) after application of Thévenin theorem to the input circuit composed of v_{sig}, R_{sig}, and R_B.

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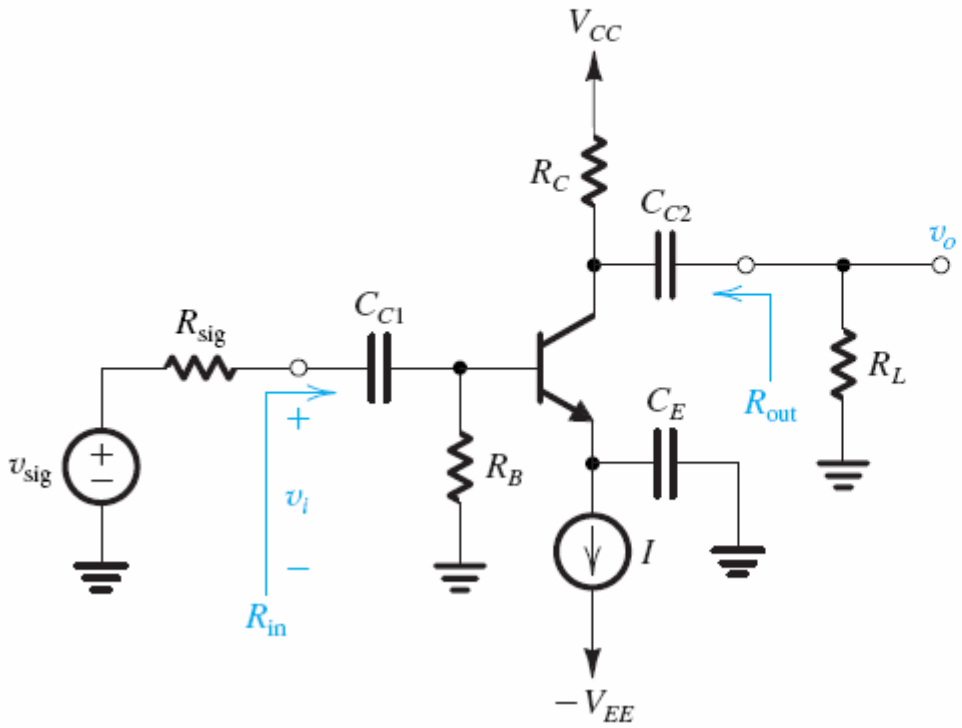
TABLE 5.6 Characteristics of Single-Stage Discrete BJT Amplifiers

Common Emitter



$$R_{in} = R_B \| r_\pi = R_B \| (\beta + 1) r_e$$

$$A_v = -g_m (r_o \| R_C \| R_L)$$

$$R_{out} = r_o \| R_C$$

$$G_v = -\frac{(R_B \| r_\pi)}{(R_B \| r_\pi) + R_{sig}} g_m (r_o \| R_C \| R_L)$$

$$\cong -\frac{\beta (r_o \| R_C \| R_L)}{r_\pi + R_{sig}}$$

$$A_{is} = -g_m R_{in} \cong -\beta$$

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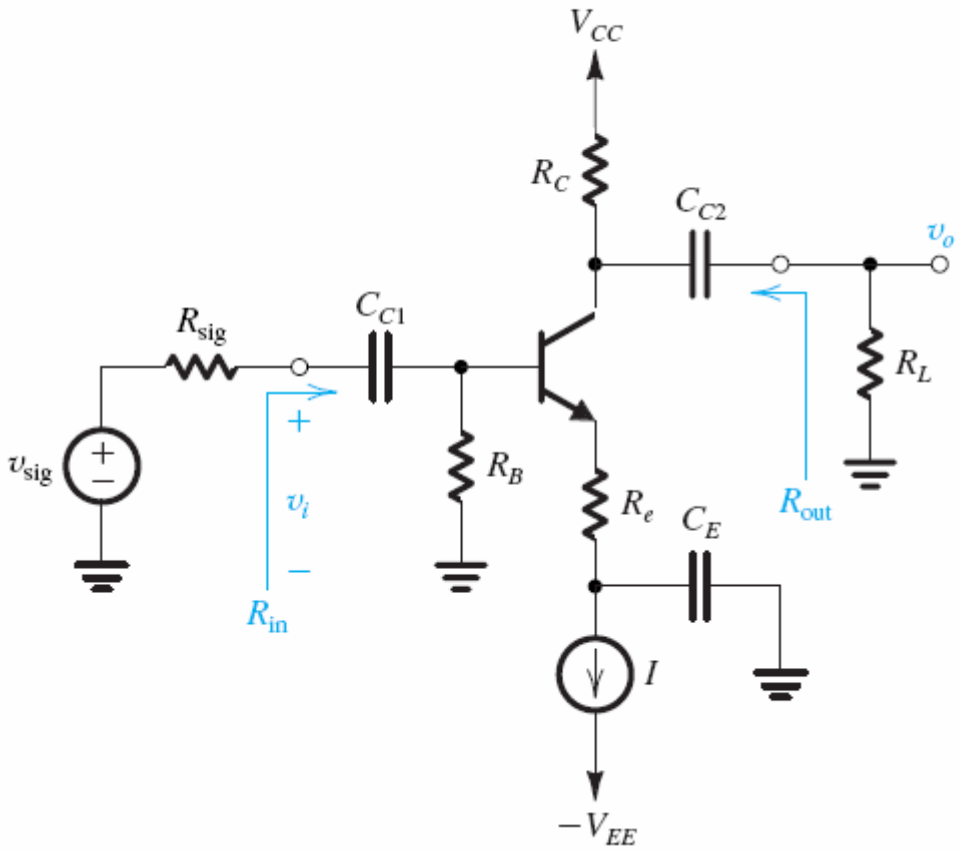
Common Emitter with Emitter Resistance



Neglecting r_o:

$$R_{in} = R_B \| (\beta + 1)(r_e + R_e)$$

$$A_v = -\frac{\alpha(R_C \| R_L)}{r_e + R_e} \cong \frac{-g_m(R_C \| R_L)}{1 + g_m R_e}$$

$$R_{out} = R_C$$

$$G_v \cong -\frac{\beta(R_C \| R_L)}{R_{sig} + (\beta + 1)(r_e + R_e)}$$

$$\frac{v_\pi}{v_i} \cong \frac{1}{1 + g_m R_e}$$

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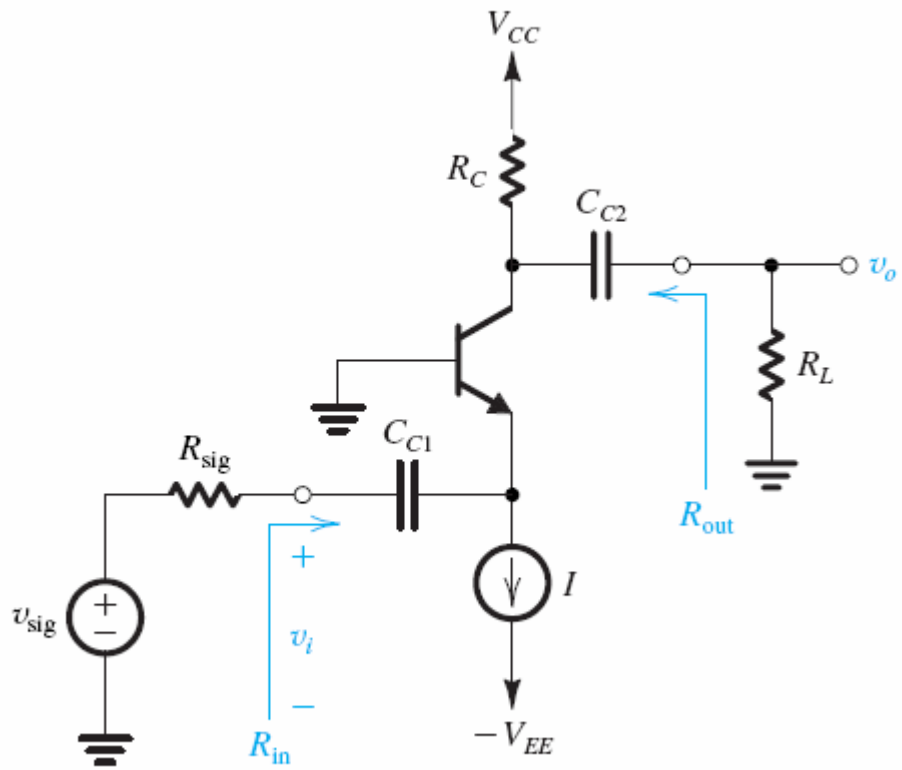
Common Base



Neglecting r_o:

$$R_{in} = r_e$$

$$A_v = g_m(R_C \parallel R_L)$$

$$R_{out} = R_C$$

$$G_v = \frac{\alpha(R_C \parallel R_L)}{R_{sig} + r_e}$$

$$A_{is} \cong \alpha$$

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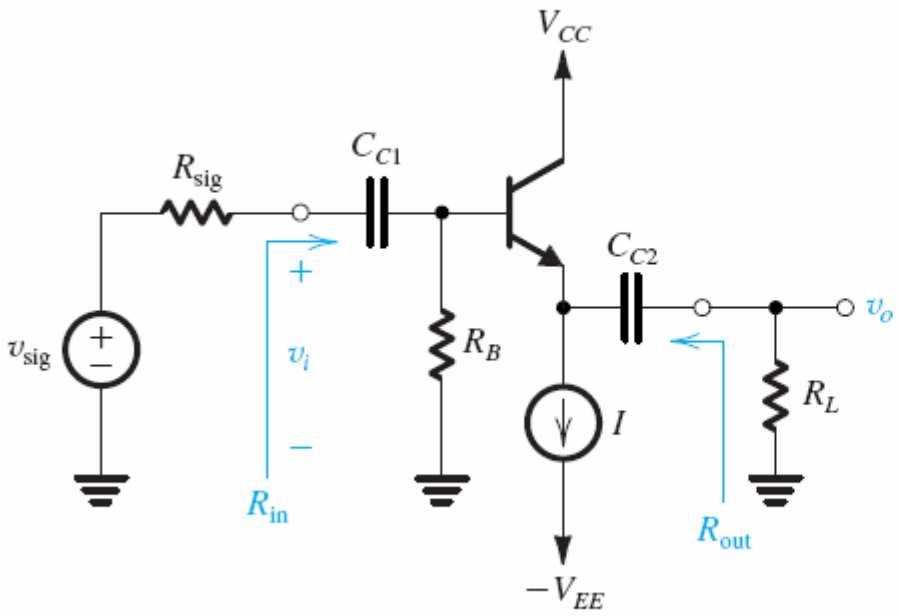
Common Collector or Emitter Follower



$$R_{in} = R_B \| (\beta + 1)[r_e + (r_o \| R_L)]$$

$$A_v = \frac{(r_o \| R_L)}{(r_o \| R_L) + r_e}$$

$$R_{out} = r_o \| \left[r_e + \frac{R_{sig} \| R_B}{\beta + 1} \right]$$

$$G_v = \frac{R_B}{R_B + R_{sig}} \frac{(r_o \| R_L)}{\frac{R_{sig} \| R_B}{\beta + 1} + r_e + (r_o \| R_L)}$$

$$A_{is} \cong \beta + 1$$

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5.10 THE BASIC BJT DIGITAL LOGIC INVERTER

- If the input voltage v_I is "high," at a value close to the power-supply voltage V_{CC}, representing a logic 1 in a positive-logic system, the transistor will be conducting and, with appropriate choice of values for R_B and R_C, saturated.
- Thus the output voltage will be $V_{CE\text{sat}} \cong 0.2$ V, representing a "low" or logic 0. Conversely, if the input voltage is "low," at a value close to ground (e.g., $V_{CE\text{sat}}$), then the transistor will be cut off, iC will be zero, and $v_O = V_{CC}$, which is "high" or logic 1.

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