

Figure 23.2 A Basic Two-Stage CMOS Op Amp. Three CD4007 arrays (A, B, C) are required. Pin numbers are for the corresponding package. Note the 6 substrate connections, which are essential for correct operation of the arrays

## E1.1 DC Operation

- Assemble the circuit shown in Fig. 23.2 using ±8 V supplies, R<sub>1</sub> = 220kΩ, R<sub>2</sub> = 1 M, and C<sub>2</sub> = 1 pF.
   Connect the positive input (A) to ground, the negative input (B) to the output (F), and a capacitor C<sub>1</sub>
   = 0.1µF from output (F) to ground.
- 有些情況下,特別是在COMS的電路,電路會在高頻產生負電阻(negative resistor), 所以量調訊號時,要申聯一個正電阻來抵消負電阻,才能量到真正的值。
   Using your DVM with a series 10 kΩ resistor as a probe (See Appendix E13), measure dc voltages at nodes A through G.

## E2.0 AC Unity-Gain Operation

## E2.1 Over-Compensated Operation with a Dominant Load Pole

- Connect the circuit of Fig. 23.2 as indicated in Exploration E1.1 above, but with input A connected to
  a waveform generator (node Λ), via a resistor, R<sub>s</sub> = 10 kΩ. Using your (normalized) dual-channel
  oscilloscope, and a 4 Vpp input square wave at 100 Hz, compare the waveforms at A and F.
   Sketch the waveforms at A and F.
- With conditions otherwise the same as in the previous step, change the generator input to a sine wave and measure the voltage gain by comparing peak-to-peak values. Now, raise the input frequency until the gain is 0.707 of its lower-frequency value (that is, until it has dropped by 3dB).