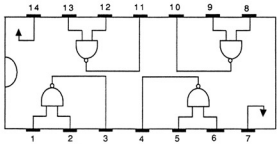


Figure 30.1 The 4011-Type Quad 2-Input NAND Package

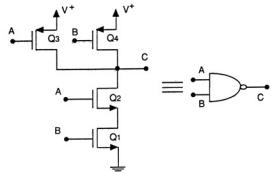


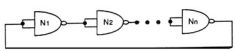
Figure 30.2 The Basic CMOS NAND Circuit

E1.1 The NAND Logic Function

- With 5 V supplied to IC pin 14, and pin 7 grounded, and with a DVM connected to node *C* (pin 3), apply all possible combinations of ground and +5V connections (4 of them) to inputs *A*, *B* (pins 1, 2). Prepare a truth table with columns *A*, *B*, *C* and entries of 0 and 5 (volts).

** - Join corresponding inputs of all four gates (all nodes *A* (pins 1, 6, 8, 13), and all nodes *B* (pins 2, 5, 9, 12)). Now run through all four input combinations, noting the corresponding output voltages at all four outputs (nodes *C* (nodes 3, 4, 10, 11)).

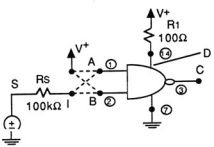
E1.2 Measurement of Propagation Delay



- Connect three of the NAND gates, with inputs joined, in a ring of 3, with the 4th NAND disabled with 1 input grounded. Using ×10 probes, connect one channel of your oscilloscope to 1 of the gate outputs and the other to the next output along the ring.

* - Please sketch the waveform and observe the phase relation to find possible **delays**

E2.0 Graphical Characterization



E2.1 Input, Transfer and Supply-Current Characterization

- With a 5 V supply voltage and 12 Vpp triangle-wave input at 1 kHz, connect inputs *A* and *B* together (pins 1, 2) to node *I*, and display voltages at nodes *A* and *C* in turn. Sketch and label the displays.

Please find Vth.

E3.1 電路設計

- use chip of 4011 to implement NOT, AND, OR gate.